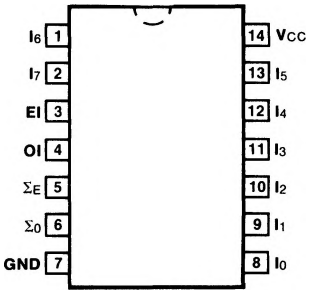
54/74180

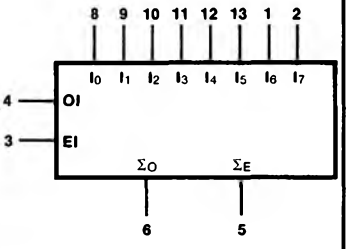
8-BIT PARITY GENERATOR/CHECKER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '180 is a monolithic, 8-bit parity checker/generator which features control inputs and even/odd outputs to enhance operation in either odd or even parity applications. Cascading these circuits allows unlimited word length expansion. Typical application would be to generate and check parity on data being transmitted from one register to another. Typical power dissipation is 170 mW.

LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V, ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74180PC		9A
Ceramic DIP (D)	A	74180DC	54180DM	6A
Flatpak (F)	A	74180FC	54180FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

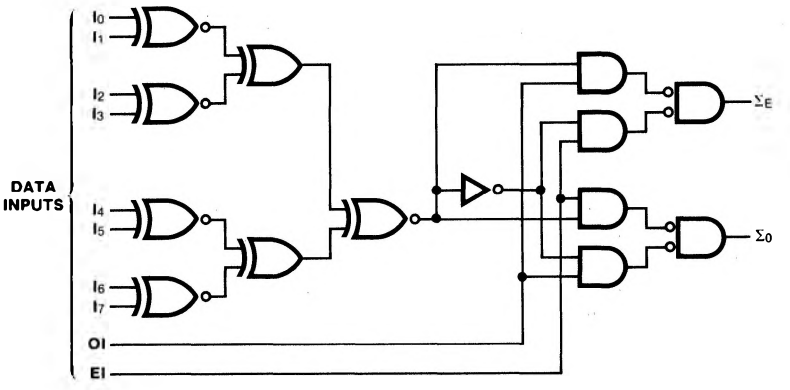
PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
I0 — I7	Data Inputs	1.0/1.0
OI	Odd Input	2.0/2.0
EI	Even Input	2.0/2.0
ΣO	Odd Parity Output	20/10
ΣE	Even Parity Output	20/10

TRUTH TABLE

INPUTS			OUTPUTS	
Σ OF 1's AT 0 THRU 7	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	H	L	H	L
ODD	H	L	L	H
EVEN	L	H	L	H
ODD	L	H	H	L
X	H	H	L	L
X	L	L	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current	XM	-20	-55	mA	V_{CC} = Max
		XC	-18	-55		
I_{CC}	Power Supply Current	XM		49	mA	V_{CC} = Max, I_n = Open OI, EI = 4.5 V
		XC		56		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF R_L = 400 Ω Min	54/74 C_L = 15 pF R_L = 400 Ω Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay I_n to Σ_E		60 68	ns	Figs. 3-1, 3-5 OI = Gnd
t_{PLH} t_{PHL}	Propagation Delay I_n to Σ_O		48 38	ns	Figs. 3-1, 3-4 OI = Gnd
t_{PLH} t_{PHL}	Propagation Delay I_n to Σ_E		48 38	ns	Figs. 3-1, 3-5 EI = Gnd
t_{PLH} t_{PHL}	Propagation Delay I_n to Σ_O		60 68	ns	Figs. 3-1, 3-4 EI = Gnd
t_{PLH} t_{PHL}	Propagation Delay EI or OI to Σ_E		20 10	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay EI or OI to Σ_O		20 10	ns	Figs. 3-1, 3-4