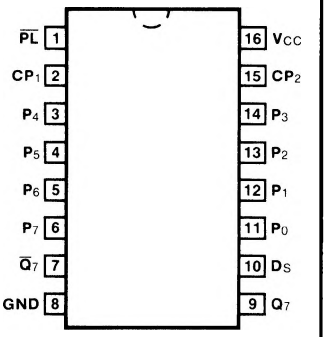
54/74165
54LS/74LS165
8-BIT PARALLEL-TO-SERIAL CONVERTER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '165 is an 8-bit parallel load or serial-in register with complementary outputs available from the last stage. Parallel inputing occurs asynchronously when the Parallel Load ($\overline{PL}$) input is LOW. With $\overline{PL}$ HIGH, serial shifting occurs on the rising edge of the clock; new data enters via the Serial Data (D_S) input. The 2-input OR clock can be used to combine two independent clock sources, or one input can act as an active LOW clock enable.

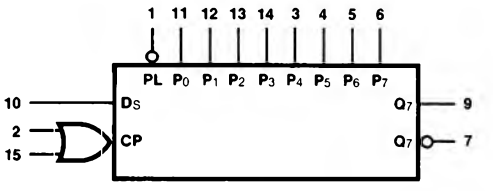
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74165PC, 74LS165PC		9B
Ceramic DIP (D)	A	74165DC, 74LS165DC	54165DM, 54LS165DM	6B
Flatpak (F)	A	74165FC, 74LS165FC	54165FM, 54LS165FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
CP_1, CP_2	Clock Pulse Inputs (Active Rising Edge)	1.0/1.0	0.5/0.25
D_S	Serial Data Input	1.0/1.0	0.5/0.25
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	2.0/2.0	1.5/0.75
P_0 — P_7	Parallel Data Inputs	1.0/1.0	0.5/0.25
Q_7	Serial Output From Last Stage	20/10	10/5.0 (2.5)
$\overline{Q}_7$	Complementary Output	20/10	10/5.0 (2.5)

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — The '165 contains eight clocked master/slave RS flip-flops connected as a shift register with auxiliary gating to provide overriding asynchronous parallel entry. Parallel data enters when the $\overline{PL}$ signal is LOW. The parallel data can change while $\overline{PL}$ is LOW provided that the recommended setup and hold times are observed.

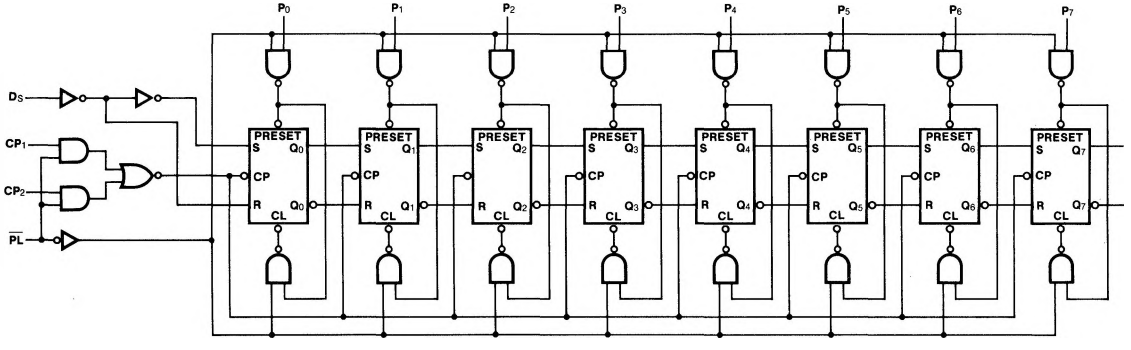
For clocked operation, $\overline{PL}$ must be HIGH. The two clock inputs perform identically; one can be used as a clock inhibit by applying a HIGH signal. To avoid double clocking, however, the inhibit signal should only go HIGH while the clock is HIGH. Otherwise, the rising inhibit signal will cause the same response as a rising clock edge. The flip-flops are edge-triggered for serial operations. The serial input data can change at any time, provided only that the recommended setup and hold times are observed, with respect to the rising edge of the clock.

TRUTH TABLE

	CP		CONTENTS								RESPONSE
$\overline{PL}$	1	2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	X	X	P_0	P_1	P_2	P_3	P_4	P_5	P_6	P_7	Parallel Entry
H	L	↓	D_S	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Right Shift
H	H	↓	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	No Change
H	↓	L	D_S	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Right Shift
H	↓	H	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	No Change

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current	XM	-20	-55			mA	V_{CC} = Max
		XC	-18	-55				
I_{CC}	Power Supply Current			63		36	mA	V_{CC} = Max, $\overline{PL}$ = ⌐⌐ P_n = ⌐ CP_1, CP_2 = 4.5 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
f_{max}	Maximum Clock Frequency	20		30		MHz	Figs. 3-1, 3-8
t_{PLH}	Propagation Delay		31		30	ns	Figs. 3-1, 3-16
t_{PHL}	$\overline{PL}$ to Q_7 or $\overline{Q}_7$		40		30		
t_{PLH}	Propagation Delay		24		30	ns	Figs. 3-1, 3-8
t_{PHL}	CP_1 to Q_7 or $\overline{Q}_7$		31		30		
t_{PLH}	Propagation Delay		17		25	ns	Figs. 3-1, 3-5
t_{PHL}	P_7 to Q_7		36		30		
t_{PLH}	Propagation Delay		27		30	ns	Figs. 3-1, 3-4
t_{PHL}	P_7 to $\overline{Q}_7$		27		25		

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
t_s (H)	Setup Time HIGH or LOW	10		10		ns	Fig. 3-13
t_s (L)	P_n to $\overline{PL}$	10		10			
t_h (H)	Hold Time HIGH or LOW	0		5.0		ns	
t_h (L)	P_n to $\overline{PL}$	0		5.0			
t_s (H)	Setup Time HIGH or LOW	20		10		ns	Fig. 3-6
t_s (L)	D_S to CP_n	20		10			
t_h (H)	Hold Time HIGH or LOW	0		5.0		ns	
t_h (L)	D_S to CP_n	0		5.0			
t_s (H)	Setup Time HIGH CP_1 to CP_2 or CP_2 to CP_1	30		30		ns	
t_w (H)	CP_n Pulse Width HIGH	25		20		ns	Fig. 3-8
t_w (L)	$\overline{PL}$ Pulse Width LOW	15		15		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{PL}$ to CP_n	45		15		ns	