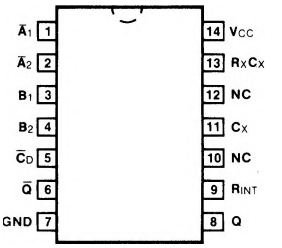
54/74122

RETRIGGERABLE RESETTABLE MULTIVIBRATOR

CONNECTION DIAGRAM
PINOUT A

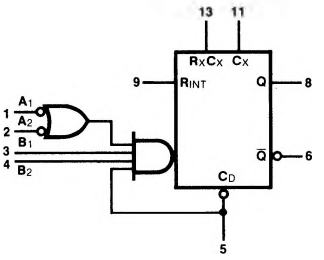


DESCRIPTION — The '122 features positive and negative dc level triggering inputs, complementary outputs, an optional 10 kΩ internal timing resistor and an overiding Direct Clear ($\overline{C}_D$) input. When the circuit is in the quasi-stable (delay) state, another trigger applied to the inputs (per Truth Table) will cause the delay period to start again, without disturbing the outputs. This process can be repeated indefinitely and thus the output pulse period (Q HIGH, $\overline{Q}$ LOW) can be made as long as desired. Alternatively, a delay period can be terminated by a LOW signal applied to $\overline{C}_D$, which also prevents triggering. An internal connection from $\overline{C}_D$ to the input gate makes it possible to trigger the circuit by a positive-going signal on $\overline{C}_D$, as shown in the Truth Table. For timing capacitor values greater than 1000 pF, the output pulse width is defined as follows:

$$t_w = 0.32\ R_X C_X\ (1.0 + 0.7/R_X)$$

Where t_w is in ns, R_X is in kΩ and C_X is in pF.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7
NC = Pins 10, and 12

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V, ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74122PC		9A
Ceramic DIP (D)	A	74122DC	54122DM	6A
Flatpak (F)	A	74122FC	54122FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

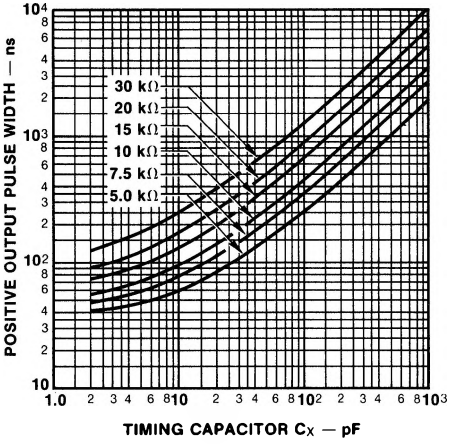
PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
$\overline{A}_1$, $\overline{A}_2$	Trigger Inputs (Active Falling Edge)	1.0/1.0
B_1, B_2	Trigger Inputs (Active Rising Edge)	1.0/1.0
$\overline{C}_D$	Direct Clear Inputs (Active LOW)	2.0/2.0
Q, $\overline{Q}$	Outputs	20/10

TRIGGERING TRUTH TABLE

INPUTS*					RESPONSE
$\overline{C}_D$	$\overline{A}_1$	$\overline{A}_2$	B_1	B_2	
L	X	X	X	X	No Trigger
X	↘	L	X	X	No Trigger
X	↘	X	L	X	No Trigger
H	↘	H	H	H	Trigger
X	X	X	↗	L	No Trigger
X	H	H	↗	X	No Trigger
H	L	X	↗	H	Trigger
↗	L	X	H	H	Trigger

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
*Input pins 1 and 2 are logically interchangeable, as are input pins 3 and 4.

PULSE WIDTH vs R_X AND C_X



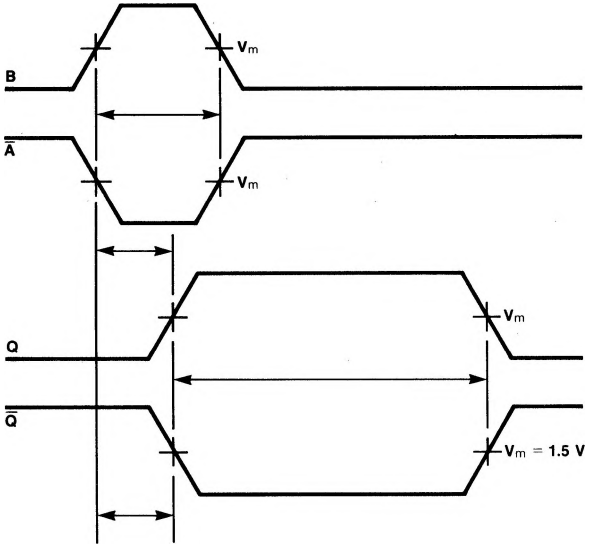


Fig. a

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74 Min	54/74 Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current	-10	-40	mA	V_{CC} = Max
I_{CC}	Power Supply Current		28	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 C_L = 15 pF, R_L = 400 Ω Max	UNITS	CONDITIONS
t_{PLH}	Propagation Delay B to Q		28	ns	C_X = 0 pF, R_X = 5 kΩ Fig. 3-1, Fig. a
t_{PLH}	Propagation Delay $\overline{A}_n$ to Q		33	ns	
t_{PHL}	Propagation Delay B to $\overline{Q}$		36	ns	
t_{PHL}	Propagation Delay $\overline{A}_n$ to $\overline{Q}$		40	ns	
t_{PLH}	Propagation Delay $\overline{C}_D$ to $\overline{Q}$		40	ns	C_X = 0 pF, R_X = 5 kΩ Figs. 3-1, 3-10
t_{PHL}	Propagation Delay $\overline{C}_D$ to Q		27	ns	
$t_{w(out)}$	Pulse Width at Q with Zero Timing Capacitor		65	ns	C_X = 0 pF, R_X = 5 kΩ Fig. 3-1, Fig. a
$t_{w(out)}$	Pulse Width with External Timing Components	3.08	3.76	μs	C_X = 1000 pF, R_X = 10 kΩ Figs. 3-1, Fig. a

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
t_w	Trigger Pulse Width		40		ns	Over Operating V_{CC} and Temperature Range
R_X	External Timing Resistor	XC	5.0	50	kΩ	
		XM	5.0	25		
C_X	External Timing Capacitor		No Restrictions		pF	