3925

ADVANCED DATASHEET –-3/31/03
(Subject to change without notice)

AUTOMOTIVE POWER MOSFET CONTROLLER

36-pin QSOP Pkg. (LQ) or
44-pin PLCC Pkg. (ED)

ABSOLUTE MAXIMUM RATINGS

Load Supply Voltages, V_{BAT}, V_{DRAIN} , V_{SW}
…… **–0.6 to 60 V**
Logic Supply Voltage, V_{DD} ……**-0.3 to 6.5 V**
Logic Input/Output, , CSOUT, VDSTH
……**-0.3 to 6.5 V**
Pins CSP, CSN, LSS ..... ***-4 to 6.5 V***
Pins SA/SB/SC…….. ……. ***-4 to 60 V***
Pins GLA/GLB/GLC…… …… ***-4 to 16 V***
Pins GHA/GHB/GHC ……. ***.-4 to 75 V***
Pins CA/CB/CC ……..…… **-0.6 to 75 V**

Package Thermal Impedance (at T_A = +25°C)
Θ_{JA} (LQ)……**44 °C/W ***
Θ_{JA} (ED) …… **23 °C/W ***

Operating Ambient Temperature Range,
T_A …….. **-40 °C to +135 °C**
Operating Junction Temperature Range,
T_J ..... **-40 °C to +150 °C**
Storage Temperature Range,
T_S..... **-55 °C to +150 °C**

** Using JEDEC Hi-K board.*

The A3925 is designed for 42-volt automotive applications that require high-power motors. The A3925 provides six, high current, gate drive outputs capable of driving a wide range of power, N-channel MOSFETs.

A requirement of automotive systems is steady operation over a varying battery input range. Bootstrap capacitors are utilized to provide the above battery supply voltage required for N-channel FETs.

Direct control of each gate output is possible via 6 TTL compatible inputs. A differential amplifier with two Sample/Hold outputs is integrated to allow accurate measurement of the low-side current in a three-phase bridge.

Diagnostic outputs can be continuously monitored to protect the driver from short-to-battery, short-to-supply, bridge-open, all under-voltage conditions, and Thermal Shutdown.

FEATURES

- Drives Wide Range of N-ch MOSFET's in 3-phase bridges
- Bootstrap circuits for high-side gate drivers
- Two, Sample/Hold Current Monitor Outputs
- Two, Diagnostic Fault Outputs
- Motor Lead Short-to-Battery, Short-to-Ground, and Bridge-open Protection
- Under-voltage Protection on all voltages
- -40°C to 135°C, T_A Operation
- Thermal Shutdown

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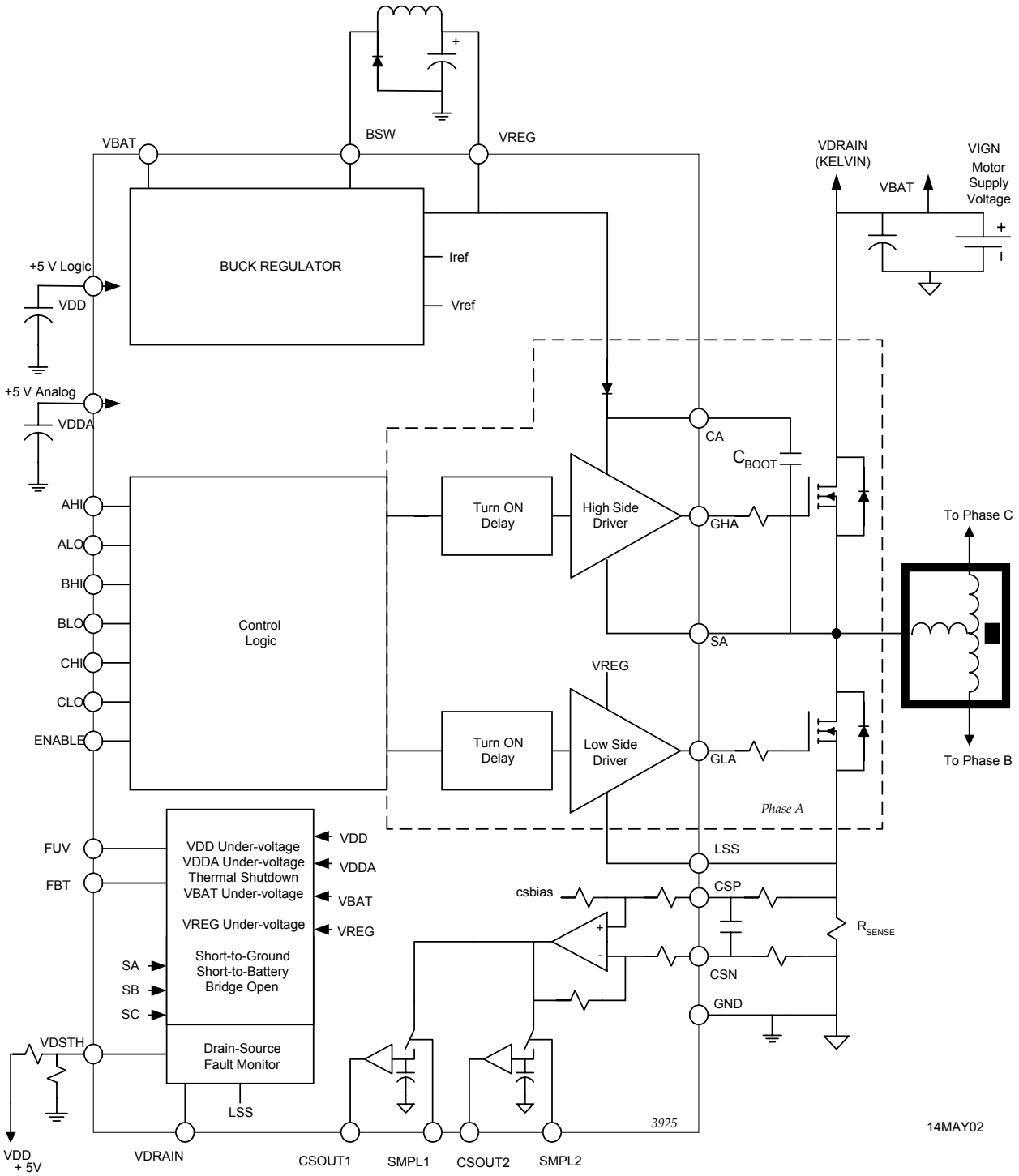
Functional Block Diagram (1 of 3 outputs shown)



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Pin Descriptions

AHI/BHI/CHI. Direct control of high-side gate outputs GHA/GHB/GHC. Logic "1" drives the gate "on". Logic "0" pulls the gate down, turning off the external power MOSFET. Internally pulled down when pin is open.

ALO/BLO/CLO. Direct control of low-side gate outputs GLA/GLB/GLC. Logic "1" drives the gate "on". Logic "0" pulls the gate down, turning off the external power MOSFET**.** Internally pulled down when pin is open.

CA/CB/CC. High-side connection for bootstrap capacitor, positive supply for high-side gate drive. The bootstrap capacitor is charged to VREG when the output Sx terminal is Low. When the output swings High, the voltage on this pin rises with the output to provide the boosted gate voltage needed for N-channel power MOSFETs.

CSN. Input for current-sense, differential amplifier, inverting, negative side. Kelvin connection for ground side of current-sense resistor.

CSOUT 1, 2. Sample/hold buffer amplifiers' output voltages proportional to current sensed across an external low-value resistor placed in the ground-side of the power FET bridge.

CSP. Input for current sense differential amplifier, non-inverting, positive side. Connected to positive side of sense resistor.

ENABLE. Logic "0" disables the gate control signals and switches off all the gate drivers. Can be used in conjunction with the gate inputs to PWM the load current. Internally pulled down when pin is open.

FUV. Logic "1" means that VBAT or VREG Under-voltage has occurred. If FUV is in Hi-Z State, then a Thermal shutdown or VDD or VDDA Under-voltage has occurred.

FBT. Logic "1" means that VBAT Under-voltage or motor/bridge fault has occurred. If FBT is in Hi-Z State, then a Thermal shutdown or VDD or VDDA Under-voltage has occurred.

GHA/GHB/GHC. High-side gate drive outputs for N-ch MOSFET drivers. External series gate resistors can control slew rate seen at the power driver gate; thereby, controlling the di/dt and dv/dt of Sx outputs.

GLA/GLB/GLC. Low-side gate drive outputs for external, N-ch MOSFET drivers. External series gate resistors can control slew rate

GND. Ground or negative side of all power supplies.

LSS. Low-Side gate driver returns. Connects to the common sources in the low-side of the power MOSFET bridge.

SA/SB/SC. Directly connected to the motor terminals, these pins sense the voltages switched across the load and are connected to the negative side of the bootstrap capacitors. Also, are the negative supply connection for the floating, high-side drivers.

SMPL 1, 2. Sample/Hold control logic inputs. Logic "1" connects internal sense amplifier output to the designated hold capacitor. Logic "0" disconnects internal sense amplifier output from that hold capacitor. Internally pulled down when pin is open.

VBAT. Battery Voltage, positive input and is usually connected to the motor voltage supply.

VDD. Logic Supply, positive side. Nominally, +5 V.

VDDA. Analog Supply, positive side. Nominally, +5 V.

VDRAIN. Kelvin connection for drain-to-source voltage monitor and is connected to high-side drains of MOSFET bridge. High-Z when pin is open and registers as a Short-to-Ground Fault on all motor phases.

VDSTH. A positive, DC level that sets the drain-to-source monitor threshold voltage. Internally pulled down when pin is open.

VREG. High-side, gate-driver supply, nominally, 13.5V.

BSW. Buck regulator output switch.

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ELECTRICAL CHARACTERISTICS **(Unless noted, otherwise: -40°C < Ta < 135°C, -40°C < T_j < 150°C, 18V < V_{BAT} < 60V, 4.75V < V_{DD} < 5.25V, Creg = 10 uF, Lreg = 330 uH, CSOUT load = 1K and 10 pF in series, CSN = gnd. (*) is design info, not tested, but guaranteed by characterization. Typical is sim. at 25°C, Max/Min are sim. over temp. range. Neg. current flows out of designated pin.)**

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Power Supplies						
Vdda Analog Supply Current	Idda	All sample and logic inputs = 0 V.			5	mA
V_{DD} Supply Current	I_{DD}	All logic inputs = 0 V.			5.2	mA
V_{BAT} Supply Current	I_{BAT}	All logic inputs = 0 V.			3	mA
VREG Avg Output Voltage	V_{REG}	0 < Ireg < 40 mA,	13	13.6	14.2	V
VREG Output Ripple *	Vreg	*Ireg=40 mA, Rlreg=0.75ohm, Rcreg=0.25ohm*	-	60	-	mV/pp
Switch ON Resistance	Rbkon	Ibk = 80 mA		8.2		Ω
Peak Switch Currents	Ibk			160		mA
Gate Drive Avg. Supply Current *	I_{REG}	No external DC load at Vreg.			40	mA
Off-time	*Toff*	*Ireg = 40 mA.*	*2.5*	*3.5*	*4.5*	*uS*
Start-up Time (to 10% of final Vreg) *	Tstartup	From VbatUV . All logic inputs = 0			*2.5*	mS
Control Logic						
Logic Input Voltages	V_{IN} (1)	Minimum high level input for logical “one”.	2.0	–	–	V
	V_{IN} (0)	Maximum low level input for logical “zero”.	–	–	.8	V
Logic Input Currents	I_{IN} (1)	V_{IN} = V_{DD}	–		500	µA
	I_{IN} (0)	V_{IN} = 0.8 V	100			µA
Input Hysteresis	V_{HYS}		100		*300*	mV
Logic Output High Voltage	V_{OH}	I_{OH} = -800µA	V_{DD}-.8			V
Logic Output Low Voltage	V_{OL}	I_{OL} = 1.6mA			.4	V

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Gate Drives, GHx, GLx (internal SOURCE or upper switch stages)						
Output HIGH Voltage	V_{DSL}(HI)	GHx: I_{xU} = -10 mA, Vsx= -Vd	V_{REG} – 2.26		V_{REG}+Vd	V
		GLx: I_{xU} = -10 mA, Vlss=0	V_{REG} – 0.26		V_{REG}	V
Source Current (pulsed)	Δ Ixu	V_{SDU} = 10 V, Tj = 25 °C, between phases		140		mA
	Ixu	V_{SDU} = 10 V, Tj = 25 °C		1.4		A
		V_{SDU} = 10 V, Tj = 135 °C	800			mA
Source ON Resistance	R_{SDU}(ON)	I_{xU} = -150 mA, Tj = 25 °C	2		8	Ω
		I_{xU} = -150 mA, Tj = 135 °C	5		13	Ω
Source Load Rise-time (20 – 80%)	Trise	Measure Vdsl, Cload = 3300 pF.		60		nS
Gate Drives, GHx, GLx (internal SINK or lower switch stages)						
Sink Current (pulsed)	Δ Ixl	V_{DSL} = 10 V, Tj = 25 °C, between phases		160		mA
	Ixl	V_{DSL} = 10 V, Tj = 25 °C		1.6		A
		V_{DSL} = 10 V, Tj = 135 ° C	1.0			A
Sink ON Resistance	R_{DSL}(ON)	I_{xL} = +150 mA, Tj = 25 °C	1		3	Ω
		I_{xL} = +150 mA, Tj = 135 ° C	1.5		4	Ω
Sink Load Fall-time (80 – 20%)	Tfall	Measure Vdsl. Cload = 3300 pF		40		nS
Gate Drives, GHx, GLx (General)						
Bootstrap Diode Forward Voltage	V_{DBOOT}	I_{DBOOT} = 10 mA	0.8		2	V
		I_{DBOOT} = 100 mA	1.5		2.3	V
Bootstrap Diode Resistance	R_{DBOOT}	R_D(100mA)=[V_D (150) -V_D (50]/100	2.5		7.5	Ω
Bootstrap Diode Current Limit	I_{LIM}	[V_{REG} – V_{CX}] = 3V	-150			mA
		[V_{REG} – V_{CX}] = 12V			*-1150*	mA
Bootstrap Quiescent Current	I_{CX}	GHx = ON,V_{CX} = 75 V, Vbat,Vsx=60V	10		30	uA
Bootstrap Refresh Time *	$t_{REFRESH}$	V_{SX} = LOW to guarantee ΔV=+0.5V refresh of 0.47 uF Boot Cap at Vcx – Vsx= +10 V.			2.0	uS
Propagation Delay, Logic only	t_{PROP}	Logic input to unloaded GHx, GLx.			150	nS
Prop Delay Differences, Logic only	t_{PROP}	Grouped by rising and falling edge transitions.			25	nS
Dead Time (Shoot-through Prevention)	t_{DEAD}	Between GHx, GLx transitions of same phase	50		150	nS

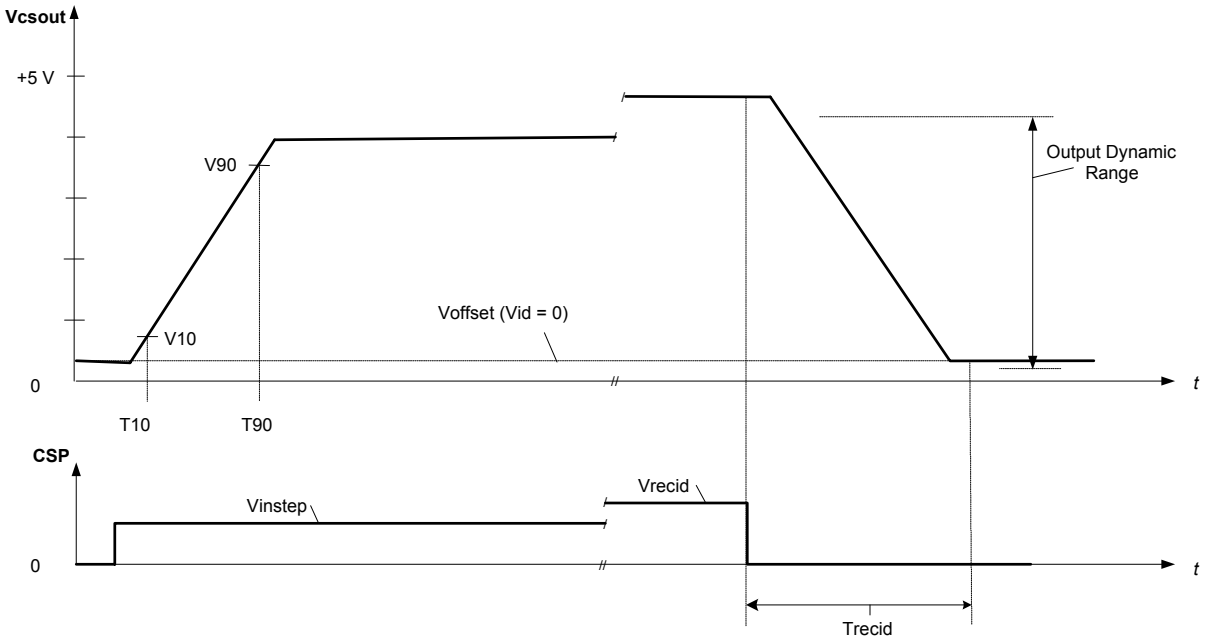
Notes: For **GH_X**: $V_{SDU} = V_{CX} - V_{GHX}$. $V_{DSL} = V_{GHX} - V_{SX}$. $V_{DSL}(HI) = V_{CX} - V_{SDU} - V_{SX}$.

For **GL_X**: $V_{SDU} = V_{REG} - V_{GLX}$. $V_{DSL} = V_{GLX} - V_{LSS}$. $V_{DSL}(HI) = V_{REG} - V_{SDU} - V_{LSS}$.

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Sense Amplifier (with one S/H Enabled)						
Input Bias Current	I_{BIAS}	CSP=CSN=0 V.	-360		-210	uA
Input Offset Current	I_{OS}	CSP=CSN=0 V.	-35		35	uA
Input Resistance	R_{IN}	CSP with respect to gnd.		80		kΩ
		CSN with respect to gnd.		4		kΩ
Diff. Input Operating Voltage	V_{ID}	V_{ID} = CSP – CSN. -1.3V < CSP,N < 4V.	0		+200	mV
Output Offset Voltage	V_{OSOUT}	CSP=CSN=0V	77	250	400	mV
Output Offset Voltage Drift *	V_{OSOUT}	CSP=CSN=0V		100		uV/°C
Input Common Mode Oper. Range	V_{CM}	CSP = CSN	-1.5		4	V
Voltage Gain	A_V	V_{ID} = 40mV to 175mV, V_{CM} in range.	18.6	19.0	19.4	V/V
Low Output Voltage Error	Verr	Vid = 0 to 40mV, Vout = 19.0*Vid + Vos + Verr	-20		+20	mV
DC Common Mode Gain	A_{CM}	CSP = CSN = 200mV			-28	dB
Source Resistance	R_{OUT}	V_{CSOUT} = 2.0 V			10	Ω
Output Dynamic Range	V_{CSOUT}	I_{CSOUT} = -100uA at top, 100uA at bottom.	0.1		V_{DA} -.3	V
Output Current (Magn.), Sink	Icssink	V_{CSOUT} = 2.0V	10			mA
Output Current,(Magn.), Source	Icssource	V_{CSOUT} = 2.0 V	2			mA
VDD, VDDA Supply Ripple Gains	PSRG	CSP=CSN=GND. Freq = 0 to 1 MHz			-20	dB
VREG Supply Ripple Gain	PSRG	CSP=CSN=GND. Freq = 0 to 300 kHz			-45	dB
Small Signal 3-dB Bandwidth *	f_{3db}	Vid = 10mv/pp		1.6		MHz
Settling Time (to within 10%)	Tsettle	CSOUT = 1.0V, set 1V/pp output sq.wave.			400	nS
AC Common Mode Gain	Acm	Vcm = 250 mV/pp, Freq = 0 to 1 MHz			-28	dB
CM Recovery Time (to within settle)	Treccm	Vcm = +4.1V to 0V step. Settle < 100 mV/pp			1	uS
Output Slew Rate	SR	Vid = 0V to +175mV, step. Meas. 10/90% pts.	10			V/us
DM Recovery Time (to within 10%)	Trecid	Vid = +250mV to 0V step. [Neg. Slew incl.]			400	nS
Sample and Hold						
Sample ON Time (to within 2 % of final value)	Tsmplon	Discharge hold (Vid=0), SMPL=OFF, sense amp to 3.0V (internally), switch SMPL=ON.			325	nS
Sample OFF Time (to within 2% of final value)	Tsmploff	With SMPL=ON, -1V/uS ramp at CSOUT. At CSOUT ~ 3.0V switch SMPL=OFF.			200	nS
Output Differences (Offsets)	Vosbuf	Vid= 0,40mV,175mV. Toggle @SMPL= 0/1/0.	-20		+20	mV
Voltage Sag	Vcsoutsg	Rate of decay of CSOUT, *SMPL = 0*	-2.5		+2.5	mV/mS

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Fault Logic						
VDD Under-voltage	V_{UVDD}	Decreasing V_{DD}	3.8		4.3	V
VDD Under-voltage Hysteresis	V_{HYSDD}	$V_{UVDD\_RECOVERY} = V_{UVDD} + V_{HYSDD}$	100		300	mV
VBAT Under-voltage	V_{UVBAT}	Decreasing V_{BAT}	14		16	V
VBAT Under-voltage Hysteresis	$V_{HYSUVBAT}$	Increasing VBAT, $V_{RECOVERY} = V_{UVBAT} + V_{HYSUVBAT}$	.8		1.6	V
VREG Under-voltage	V_{UVREG}	Decreasing VREG	9.5		10.5	V
VREG Under-voltage Hysteresis	$V_{HYSUVREG}$	Increasing VREG, $V_{RECOVERY} = V_{UVREG} + V_{HYSUVREG}$	50		200	mV
VDSTH Input Range *	V_{DSTH}		0.5		3	V
VDSTH Input Current	I_{DSTH}		50		110	uA
Short-to-Ground Threshold	V_{STG}	With a High-side driver “on”, as V_{SX} decreases, $V_{DRAIN} - V_{SX} > V_{STG}$, causes a fault.	V_{DSTH} -0.3		V_{DSTH} + 0.2	V
Short-to-Battery Threshold	V_{STB}	With a Low-side driver “on”, as V_{SX} increases, $V_{SX} - V_{LSS} > V_{STB}$, causes a fault.	V_{DSTH} -0.3		V_{DSTH} + 0.2	V
V_{DRAIN} /Open Bridge Operating Range	V_{DRAIN}		-0.3		V_{BAT}+2	V
V_{DRAIN} /Open Bridge Leakage Curr.	I (V_{DRAIN})		0	0.5	1.0	mA
V_{DRAIN} /Open Bridge Threshold Volt.	V_{BDGOTH}	If $V_{DRAIN} < V_{BDGOTH}$ then a Bridge fault occurs.	1		3	V
Thermal Shutdown Temp.	T_J		160	170	180	°C
Thermal Shutdown Hysteresis	ΔT_J		7	10	13	°C

3925 CURRENT SENSE AMPLIFIER WAVEFORMS



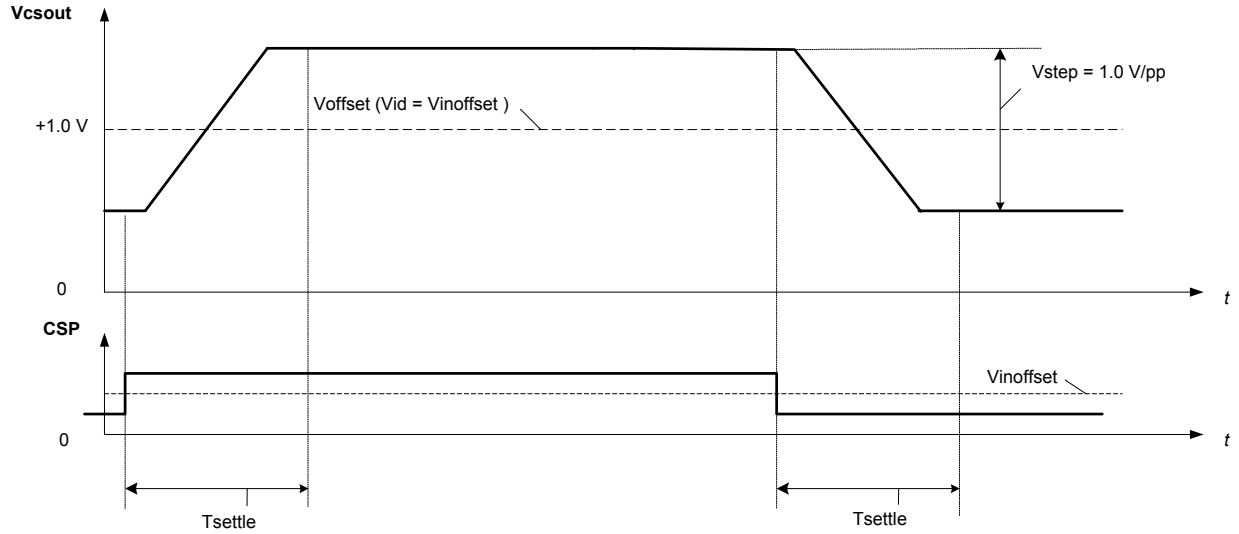


Figure 2: Small Signal Transient Response (Differential Input, CSN = 0)

3925 SAMPLE / HOLD WAVEFORMS

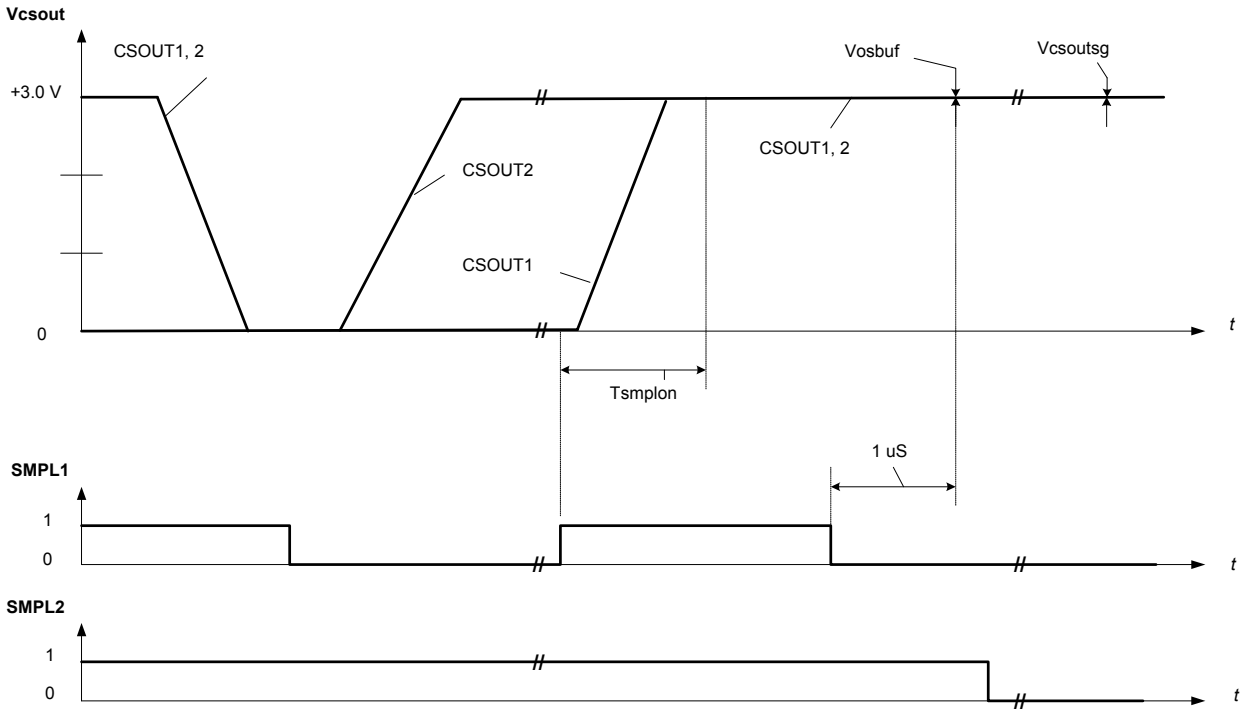


Figure 3: Sample ON Time

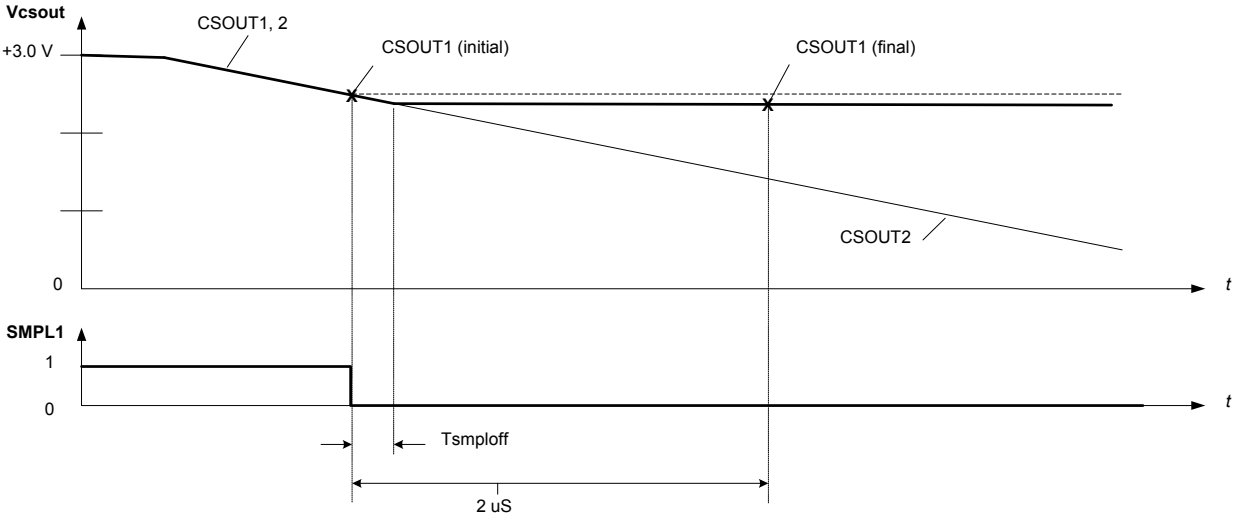


Figure 4: Sample OFF Time (SMPL2 = 1)

Functional Description

Motor Lead Protection. A fault detection circuit monitors the voltage across the drain to source of the external MOSFETs. A fault is asserted "High" on the output pin, FBT, if the voltage across the drain to source of any MOSFET that is instructed to turn on is greater than the voltage applied to the V_{DSTH} input terminal. The low-side, drain-source monitor uses the LSS pin, rather than V_{DRAIN} pin, in comparing against the V_{DSTH} voltage. The V_{DSTH} voltage is set by a resistor divider to V_{DD}.

Pin V_{DRAIN} is intended to be a Kelvin connection for the high-side, drain-source monitor circuit. Voltage drops across the power bus are eliminated by connecting a private PCB trace from the V_{DRAIN} pin to the common drains of the MOSFET bridge. This allows improved accuracy in setting the V_{DSTH} threshold voltage.

Fault Outputs. Transient faults on any of the fault outputs may occur during switching but will not disable the gate drive outputs. External circuitry or controller logic must determine if the faults represent a hazardous condition.

FBT. The FBT pin will go active "High" if a Vbat Under-voltage occurred or, if a gate is commanded to turn ON, then a Motor Lead Short-to-Ground, Motor Lead Short-to-Supply (or Battery) or Bridge (or V_{DRAIN}) Open Fault occurred.. This fault flag indicates a motor/bridge fault, primarily, but with FUV asserted means a Vbat Under-voltage occurred and the part has entered Shutdown.Along with the FUV, Hi-Z state indictes that there is an over-temperature condition (TSD) or the VDD or VDDA are under-voltage and the part has entered Shutdown.

FUV. The FUV pin will go active "High" if a V_{BAT} Under-voltage or Vreg Under-voltage fault occurred. This fault flag indicates a Voltage Fault, primarily, but with FBT asserted means a Vbat Under-voltage occurred and the part has entered Shutdown. Along with the FBT, a Hi-Z state indictes there is an over-temperature condition (TSD) or the VDD or VDDA are under-voltage and the part has entered Shutdown.

Shutdown. If a fault occurs because of excessive junction temperature or under-voltage on Vdd, Vdda, or Vbat, all gate driver outputs are driven "Low" (COAST mode) until the fault condition is removed. In addition, the buck regulator supply switch is turned "off" until the other under-voltages and the junction temperature recover.

Current Sensing. A current sense amplifier is provided to allow system monitoring of the FET bridge load current through two, selectable, sample/hold unity gain buffer output stages. The differential amplifier inputs are Kelvin connected across a low-value sense resistor or current shunt, R_{SENSE}. The output voltage is:

$$V_{CSOUT} = (I_{LOAD} * A_V * R_{SENSE}) + V_{OS}$$

where V_{OS} is output voltage calibrated at zero load current. A_V = Differential gain of sense amplifier.

VREG Regulator. A PFM Buck Regulator driven from the Vbat with internal current limit control and min.off-time, Toff. When the output voltage, Vreg, is below target, the buck switch turns on connecting Vbat to Vsw and forcing current into Lreg until it reaches the internal switch current limit value, where it turns off. Inductor current completely decays through the external, recirculation diode during the fixed Off Time. The switching cycle frequency increases as the output load current or the Vbat voltage increases.

Input Logic.

Enable	(x)LO	(x)HI	GL(x)	GH(x)	Mode of Operation
0	X	X	0	0	All gate drive outputs Low
1	0	0	0	0	All gate drive outputs Low
1	0	1	0	1	High Side On
1	1	0	1	0	Low Side On
1	1	1	0	0	All gate drive outputs Low (XOR feature)

Fault Responses.

FAULT MODE	ENABLE	FBT	FUV	VREG REG.	GH_X	GL_X
No Fault	X	0	0	ON	-	-
Short-to-Battery	1*	1	0	ON	-	-
Short-to-Ground	1*	1	0	ON	-	-
Bridge (V_{DRAIN}) Fault	1*	1	0	ON	-	-
V_{REG} Under-voltage	X	0	1	ON	-	-
V_{DD} or V_{DDA} Under-voltage or Thermal Shutdown !	X	Z	Z	OFF	0	0
V_{BAT} Under-voltage !	X	1	1	OFF	0	0

Notes: FUV = VregUV + VbatUV. FBT = EN[GHx(SG + BF) + GLx(SB)] + VbatUV.
Z = VddUV + VddaUV + TSD.
x = "little x "indicates A, B, or C phase.
X = "Capital X " indicates a "don't care".
- = Depends on (x)LO, (x)HI inputs and ENABLE.
Z = Tri-stated output.
1* = Short-to-Battery can only be detected when the corresponding GL_X = 1. Similarly, Short-to-Ground can only be detected when the corresponding GH_X = 1. Bridge Fault appears as a Short-to-Ground fault on all phases. These faults are not detected when ENABLE = 0.
! = These faults are not only reported but action is taken by the internal logic to protect this IC (shuts off the Vreg Regulator) and coast the motor.

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Terminal Lists for 36-pin QSOP (LQ) and 44-pin PLCC (ED)

36LQ, Pin #	*44ED, Pin #*	Pin Name	Pin Description
1	*15*	CSP	Current sense input, positive-side
2	*16*	VDSTH	DC Input, Drain-to-Source Monitor Threshold Voltage
3	*17*	CC	Bootstrap C Cap
4	*18*	SC	Motor Phase C Input
5	*19*	GHC	High-Side C Gate Drive Output
6	*20*	SB	Motor Phase B Input
7	*21*	GHB	High-Side B Gate Drive Output
8	*24*	CB	Bootstrap B Cap
9	*25*	SA	Motor Phase A Input
10	*26*	GHA	High-Side A Gate Drive Output
11	*27*	CA	Bootstrap A Cap
12	*28*	GLC	Low-Side C Gate Drive Output
13	*29*	GLB	Low Side B Gate Drive Output
14	*30*	GLA	Low-Side A Gate Drive Output
15	*31*	LSS	Low-Side, Gate Drive Source returns
16	*32*	VREG	Buck Reg./Gate Drive Supply Output, Positive
17	*33*	VDRAIN	Kelvin Connection to MOSFET high-side drains
18	-	GND	GROUND, Supply Returns, Negative
19	*36*	BSW	Buck Regulator Switch Output
20	*37*	VBAT	Battery Supply Connection, Positive
21	*38*	VDD	Logic Supply, Positive
22	*39*	FUV	Under-voltage Fault
23	*40*	FBT	Bridge Terminal Fault
24	*41*	ALO	Gate Control Signal, A, Low-side
25	*42*	AHI	Gate Control Signal, A, High-side
26	*43*	BHI	Gate Control Signal, B, High-side
27	*44*	BLO	Gate Control Signal, B, Low-side
28	*3*	CLO	Gate Control Signal, C, Low-side
29	*4*	CHI	Gate Control Signal, C, High-side
30	*5*	ENABLE	Gate Output Enable
31	*6*	SMPL2	Sample Gate for CSOUT2
32	*7*	CSOUT2	Current sense amplifier output after S/H 2
33	*8*	SMPL1	Sample Gate for CSOUT1
-	*9*	*TP*	*Test Point for manufacturing test use, only.*
34	*10*	CSOUT1	Current sense amplifier output after S/H 1
35	*13*	VDDA	Analog Supply. Positive
36	*14*	CSN	Current sense input, negative-side
-	*1,2,11,12,22, 23,34,35*	GND	GROUND, Supply Returns, Negative. Heat path, die attach, connected to chip GND at pin 34.