intel®

3232

# ADDRESS MULTIPLEXER AND REFRESH COUNTER FOR 4K DYNAMIC RAMs

- ■ **Ideal For 2104A**
- ■ **Simplifies System Design**
- ■ **Reduces Package Count**
- ■ **Standard 24-Pin DIP**

- ■ **Address Input to Output Delay: 9ns Maximum Driving 15pF, 25ns Maximum Driving 250pF**
- ■ **Suitable For Either Distributed Or Burst Refresh**
- ■ **Single Power Supply: +5 Volts ±10%**

The Intel® 3232 contains an address multiplexer and refresh counter for multiplexed address dynamic RAMs requiring refresh of up to 6 input addresses (or 4K bits for 64 x 64 organization). It multiplexes twelve bits of system supplied address to six output address pins. The device also contains a 6 bit refresh counter which is externally controlled so that either distributed or burst refresh may be used. The high performance of the 3232 makes it especially suitable for use with high speed N-channel RAMs like the 2104A.

The 3232 operates from a single +5 volt power supply and is specified for operation over a 0 to +75°C ambient temperature range.

PIN CONFIGURATION
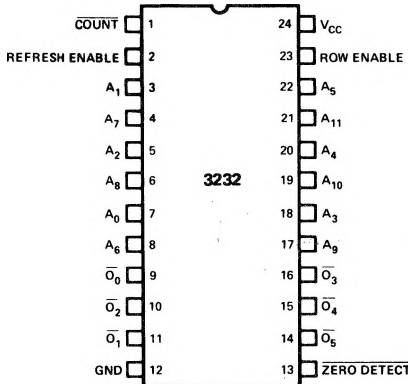
NOTE: A_0 THROUGH A_5 ARE ROW ADDRESSES.
A_6 THROUGH A_{11} ARE COLUMN ADDRESSES.

TRUTH TABLE AND DEFINITIONS:

REFRESH ENABLE	ROW ENABLE	OUTPUT
H	X	REFRESH ADDRESS (FROM INTERNAL COUNTER)
L	H	ROW ADDRESS (A_0 THROUGH A_5)
L	L	COLUMN ADDRESS (A_6 THROUGH A_{11})

COUNT – ADVANCES INTERNAL REFRESH COUNTER.
ZERO DETECT – INDICATES A ZERO IN THE REFRESH ADDRESS (USED IN BURST REFRESH MODE).

LOGIC DIAGRAM
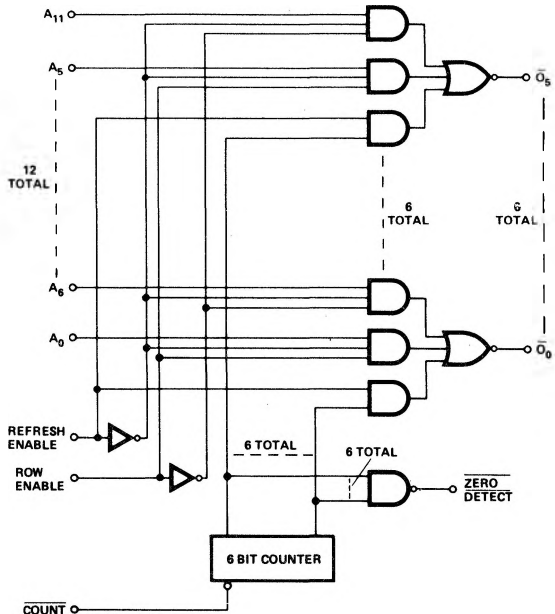
Absolute Maximum Ratings*

Temperature Under Bias .... -65° to +125°C
Storage Temperature .... -65° to +160°C
All Input, Output, or
  Supply Voltages .... -0.5V to +7 Volts
Output Currents 100mA
Power Dissipation 1W

COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

All Limits Apply for $V_{CC} = 5.0V \pm 10\%$, $T_A = 0°C$ to $+75°C$

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP. (1)	MAX.		
I_F	Input Load Current		-0.04	-0.25	mA	$V_{IN} = 0.45V$
I_R	Input Leakage Current		0	10	μA	$V_{IN} = 5.5V$
V_{IH}	Input High Voltage	2.0			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OL}	Output Low Voltage		0.25	0.40	V	$I_{OL} = 5mA$
V_{OH}	Output High Voltage ($\overline{O}_0$-$\overline{O}_5$)	2.8	4.0		V	$I_{OH} = -1mA$
V_{OHI}	Output High Voltage ($\overline{Zero\ Detect}$)	2.4	3.3		V	$I_{OH} = -1mA$
I_{CC}	Power Supply Current		100	150	mA	$V_{CC} = 5.5V$

Note 1.   Typical values are for $T_A = 25°C$ and $V_{CC} = 5.0V$.

A.C. Characteristics

All Limits Apply for V_{CC} = +5.0V ±10%, T_A = 0°C to 75°C, Load = 1 TTL, C_L = 250pF, Unless Otherwise Specified.

SYMBOL	PARAMETER	MIN.	TYP.[1]	MAX.	UNIT	CONDITIONS
t_{AO}	Address Input to Output Delay		6	9	ns	Refresh Enable = Low [1] [2]
t_{AOI}	Address Input to Output Delay		16	25	ns	Refresh Enable = Low
t_{OO}	Row Enable to Output Delay	7	12	27	ns	Refresh Enable = Low [1] [2]
t_{OOI}	Row Enable to Output Delay	12	28	41	ns	Refresh Enable = Low
t_{EO}	Refresh Enable to Output Delay	7	14	27	ns	Note 1, 2
t_{EOI}	Refresh Enable to Output Delay	12	30	45	ns	
t_{CO}	Count to Output	15	40	60	ns	Refresh Enable = High [1] [2]
t_{COI}	Count to Output	20	55	80	ns	Refresh Enable = High
f_C	Counting Frequency	5			MHz	
t_{CPW}	Count Pulse Width	35			ns	
t_{CZ}	Count to Zero Detect	15		70	ns	Note 2

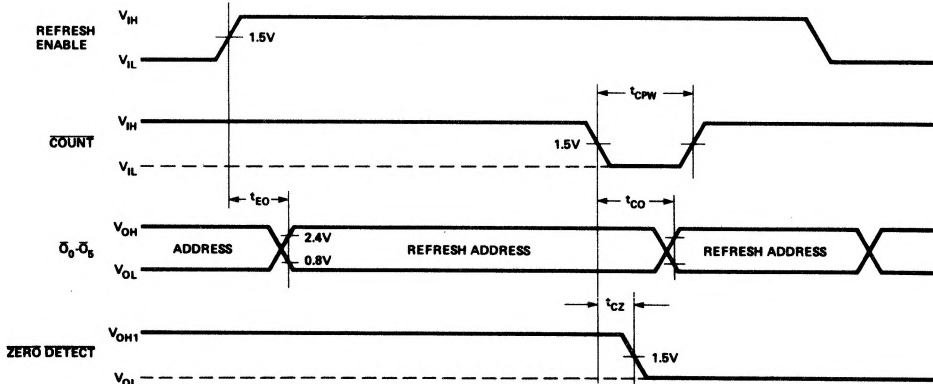Note 1: V_{CC} = 5.0V, T_A = 25°C
    2: C_L = 15pF

A.C. TIMING WAVEFORMS (Typically used with 2104A)

NORMAL CYCLE
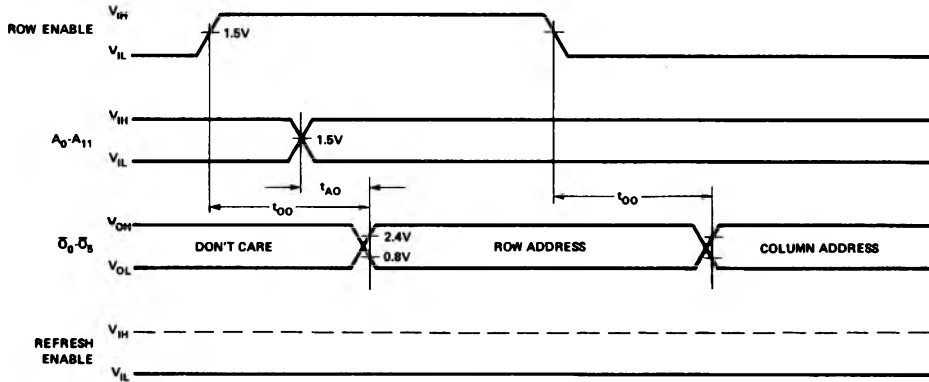
REFRESH CYCLE

PIN NAMES AND FUNCTIONS

Pin. No.	Pin Name	Function
1	$\overline{\text{Count}}$ Input	Active low input increments internal six bit counter by one for each count pulse in.
2	Refresh Enable Input	Active high input which determines whether the 3232 is in refresh mode (H) or address enable (L).
7,3,5,18, 20,22	A_0-A_5 Inputs	Row Address inputs.
8,4,6,17, 19,21	A_6-A_{11} Inputs	Column address inputs.
9,11,10, 16,15,14	$\overline{O}_0$-$\overline{O}_5$ Outputs	Address outputs to memories. Inverted with respect to address inputs.
12	GND	Power supply ground.
13	$\overline{\text{Zero Detect}}$ Output	Active low output which senses that all six bits of refresh address in the counter are zero. Can be used in the burst mode to sense refresh completion.
23	Row Enable Input	High input selects row, low input selects column addresses of the driven memories.
24	V_{CC}	+5V power supply input.

DEVICE OPERATION

The Intel® 3232 Address Multiplexer/Refresh Counter performs the following functions:

1. Row, Column and Refresh Address multiplexing
2. Address counting for burst or distributed refresh.

These functions are controlled by two signals: Refresh Enable and Row Enable, both of which are active high TTL inputs. The truth table on page 1 shows the levels required to multiplex to the output:

1. Refresh addresses (from internal counter)
2. Row addresses (A_0 through A_5)
3. Column addresses (A_6 through A_{11})

Burst Refresh Mode

When refresh is requested, the refresh enable input is high. This input is ANDed with the 6 outputs of the internal 6 bit counter. At each $\overline{\text{Count}}$ pulse the counter increments by one, sequencing the outputs ($\overline{O}_0$-$\overline{O}_5$) through all 64 row addresses. When the counter sequences to all zeros, the $\overline{\text{Zero Detect}}$ output goes low signaling the end of the refresh sequence. Due to counter decoding spikes, the $\overline{\text{Zero Detect}}$ output is valid only after t_{CZ} following the low going edge of $\overline{\text{Count}}$.

Distributed Refresh Mode

In the distributed refresh mode, one row is selected for refresh each ($t_{REFRESH}/n$) time where n = number of rows in the device and $t_{REFRESH}$ is the specified refresh rate for the device. For the 2104A $t_{REFRESH}$ = 2msec and n = 64, therefore one row is refreshed each 31 μsec. Following the refresh cycle at row n_x, the Count input is pulsed, advancing the refresh address by one row so that the next refresh cycle will be performed on row n_{x+1}. The Count input may be pulsed following each refresh cycle or within the refresh cycle after the specified memory device address hold time.

Row and Column Address

All twelve system address lines are applied to the inputs of the 3232. When Refresh Enable is low and Row Enable is high, input addresses A_0-A_5 are gated to the outputs and applied to the driven memories. Conversely, when Row Enable is low (with Refresh Enable still low), input addresses A_6-A_{11} are gated to the outputs and applied to the driven memories.

Figure 1 shows a typical connection between the 3232 and the 2104A 4K dynamic RAM. When the memory devices are driven directly by the 3232, the address applied to the memory devices is the inverse of the address at the 3232 inputs due to the inverted outputs of the 3232. This should be remembered when checking out the memory system.
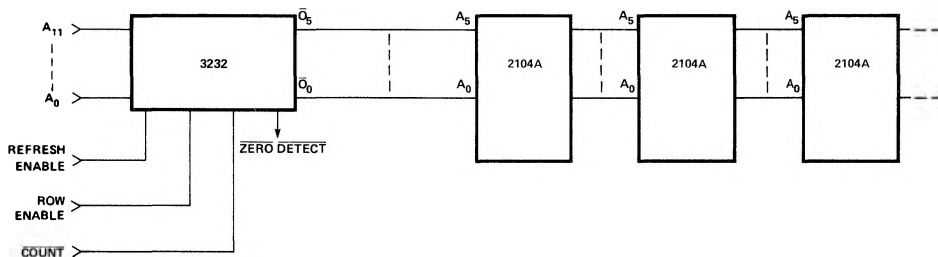

Figure 1. Typical Connection of 3232 and 2104 Memories.