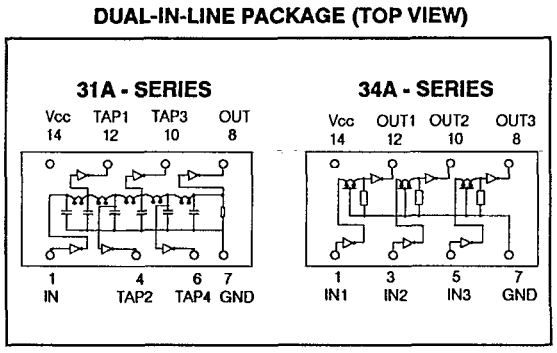
DIGITAL DELAY MODULES 31A, 34A Series
5 Tap and Triple Independent 14 Pin Moulded DIP

- ❒ Schottky TTL buffered
- ❒ 14 pin package
- ❒ Low profile
- ❒ TTL compatible
- ❒ Industry standard pin-outs

DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The 31A and 34A series of Digital Delay Modules are Schottky TTL buffered delay lines providing precise delay times and direct compatability with TTL. Five equally spaced delay taps, and triple independent equal delays are each packaged in low profile 14 pin dual-in-line configurations having industry standard pin-outs. Internal termination of the delay line and compensation for propagation delays are incorporated in the design so that no additional external components are needed. These modules are particularly suitable for high density board designs.

absolute maximum ratings over operating free-air temperature range

Supply voltage V_{cc} 7V
Input voltage 5.5V
Min. pulse width as % of total delay 80%
Input pulse repetition rate PRR . . . . . 3 x pulse width min.
Operating free-air temperature range . . . . . 0C to 70C
Storage temperature range . . . . . –55C to 125C
Temperature coefficient of delay . . . . . ± 300ppm/C
Lead temperature 1.5mm from case for 10 seconds 300C

drive capabilities

Logic 0 output . . . . . 10 TTL loads per tap max.
20 TTL loads per unit max.
Logic 1 output . . . . . 20 TTL loads per unit max.

electrical specifications over operating free-air temperature range

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{OH} High-level output voltage	V_{CC} = 4.75V V_{IH} = 2V, I_{OH} = −1mA	2.7	3.4		V
V_{OL} Low-level output voltage	V_{CC} = 4.75V I_{OL} = 20mA, V_{IL} = 0.8V			0.5	V
I_{IH} High-level input current	V_{CC} = 5.25V, V_{IH} = 2.7V			50	μA
I_{IL} Low-level input current	V_{CC} = 5.25V, V_{IL} = 0.5V			−2	mA
I_{CC} Supply current outputs high	V_{CC} = 5.25V			24	mA
I_{CC} Supply current outputs low	V_{CC} = 5.25V			54	mA

delay characteristics V_{cc} = 5V, Ta = 25C, no loads at taps, input test pulse width 100% of total delay, input rise time 3.0ns.

delay tolerance from input to tap ±2ns or ±5% whichever is greater

31A SERIES 5 Tap 14 Pin DIP
Package style H with pins 2, 3, 5, 9, 11, and 13 missing

PART No.	TOTAL DELAY (ns) ±5% (1)	TAP TO TAP DELAY (ns)	OUTPUT RISE TIME (ns)
31A - 5250	25	5 ± 2	3
31A - 5500	50	10 ± 2	3
31A - 5101	100	20 ± 2	3
31A - 5151	150	30 ± 3	4
31A - 5201	200	40 ± 4	4
31A - 5251	250	50 ± 5	4
31A - 5301	300	60 ± 6	4
31A - 5401	400	80 ± 8	4
31A - 5501	500	100 ± 10	4

Note: Delays measured at 1.5V on leading edge, Rise Time measured from 0.75V to 2.4V

(1) or ± 2ns whichever is greater

31A, 34A Series
5 Tap and Triple Independent 14 Pin Moulded DIP

34A Triple independent equal 14 Pin DIP
Package style H with pins 2, 4, 6, 9, 11 and 13 missing

PART No.	TOTAL DELAY (ns) ±5% (1)	RISE TIME (ns) max.	PART No.	TOTAL DELAY (ns) ±5% (1)	RISE TIME (ns) max.
34A - 010	10	4	34A - 060	60	4
34A - 020	20	4	34A - 070	70	4
34A - 030	30	4	34A - 080	80	4
34A - 040	40	4	34A - 090	90	4
34A - 050	50	4	34A - 100	100	4

Note: Delays measured at 1.5V on leading edge, Rise Time measured from 0.75V to 2.4V

(1) or ±2ns whichever is greater