

DESCRIPTION

The 1702A is ideally suited for uses where fast turn-around and pattern experimentation are important. The device undergoes complete programming and functional testing on each bit position prior to shipment, thus insuring 100% programmability.¹

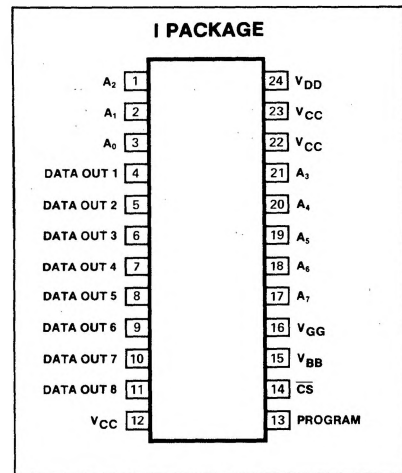
The 1702A is packaged in a 24-pin dual in-line package with a UV transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device.

The 1702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of high performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

FEATURES

- Fast programming for all 2048 bits: 2 minutes
- All 2048 bits guaranteed programmable
- 100% factory tested
- Fully decoded
- Static MOS: No clocks required
- Inputs and outputs DTL and TTL compatible
- Tri-state output: OR-tie capability
- Simple memory expansion
- Chip select input lead

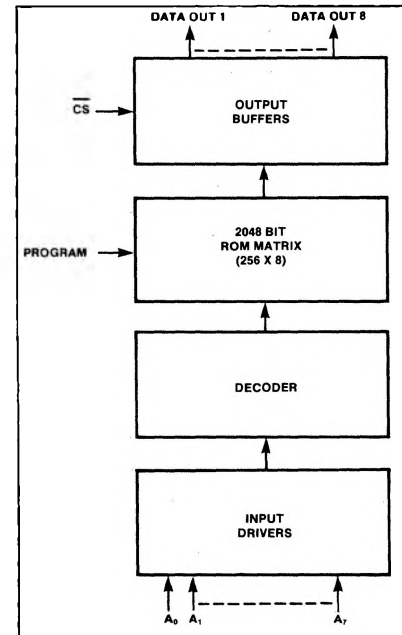
PIN CONFIGURATION



PIN DESIGNATION²

PIN NO.	SYMBOL	NAME & FUNCTION
Read mode		
12	V _{CC}	V _{CC}
13	Program	V _{CC}
14	$\overline{\text{CS}}$	GND
15	V _{BB}	V _{CC}
16	V _{GG}	V _{GG}
22	V _{CC}	V _{CC}
23	V _{CC}	V _{CC}
Programming mode		
12	V _{CC}	GND
13	Program	Program pulse
14	$\overline{\text{CS}}$	GND
15	V _{BB}	V _{BB}
16	V _{GG}	Pulsed V _{GG} (V _{IL4P})
22	V _{CC}	GND
23	V _{CC}	GND

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS³

PARAMETER	RATING	UNIT
Temperature range		
T _A Operating	0 to +70	°C
T _{STG} Storage	-65 to +125	°C
Power dissipation		
P _D	2	W
Soldering of leads (10sec)		
	300	°C
Input voltages and supply voltages with respect to V _{CC}		
Read operation	0.5 to -20	V
Program operation	-48	V

DC ELECTRICAL CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$, $V_{DD} = -9\text{V} \pm 5\%$, $V_{GG}^3 = -9\text{V} \pm 5\%$ unless otherwise specified.⁴

PARAMETER	TEST CONDITIONS	LIMITS			UNIT	
		Min	Typ	Max		
V_{IL1} V_{IL2} V_{IH}	Input voltage Low for TTL interface Low for MOS interface Address and chip select high	-1.0 V_{DD} $V_{CC}-2$		0.65 $V_{CC}-6$ $V_{CC}+0.3$	V	
V_{OL} V_{OH}	Output voltage Low High	$I_{OL} = 1.6\text{mA}$ $I_{OH} = -100\mu\text{A}$	3.5	-0.7 4.5	0.45	V
I_{LI}	Address and chip select input load current	$V_{IN} = 0.0\text{V}$			1	μA
I_{LO}	Output leakage current	$V_{OUT} = 0.0\text{V}$, $\overline{CS} = V_{CC} - 2$			1	μA
I_{DD1} I_{DD2} I_{DD3} I_{GG}	Supply current Gate	$I_{OL} = 0.0\text{mA}$ $\overline{CS} = V_{CC} - 2$, $T_A = 25^\circ\text{C}$ $\overline{CS} = 0.0$, $T_A = 25^\circ\text{C}$ $\overline{CS} = V_{CC} - 2$, $T_A = 0^\circ\text{C}$		35 32 38.5	50 46 1	mA
I_{CF1} I_{CF2} I_{OL} I_{OH}	Output current Clamp Sink Source	$V_{OUT} = -1.0\text{V}$ $T_A = 0^\circ\text{C}$ $T_A = 25^\circ\text{C}$ $V_{OUT} = 0.45\text{V}$ $V_{OUT} = 0.0\text{V}$	1.6 -2.0	8 4	14 13	mA
C_{IN} C_{OUT}	Capacitance ⁵ Input Output	All unused pins are at ac ground $V_{IN} = V_{CC}$, $\overline{CS} = V_{CC}$ $V_{OUT} = V_{CC}$, $V_{GG} = V_{CC}$		8 10	15 15	pF

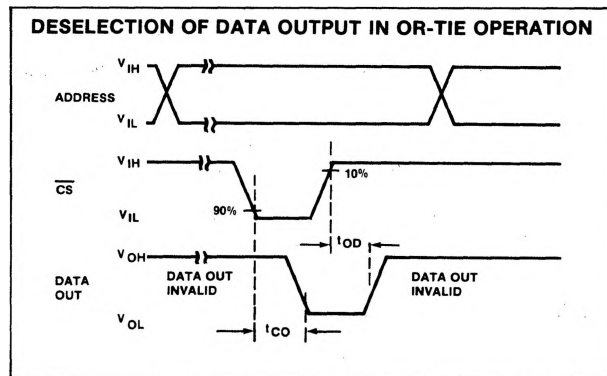
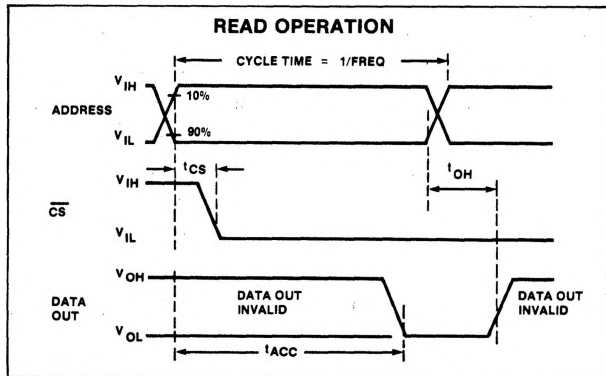
AC ELECTRICAL CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$, $V_{DD} = -9\text{V} \pm 5\%$ unless otherwise specified, Input pulse amplitudes = 0 to 4V, t_R , $t_F \leq 50\text{ns}$, Output load is 1 TTL gate, Measurements made at output of TTL gate ($t_{PD} \leq 15\text{ns}$, $C_L = 15\text{pF}$)

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ	Max	
Freq t_{OH}	Repetition Rate Previous read data valid				1 100	MHz ns
t_{ACC}^1 t_{CS} t_{CO}	Delay time Output Output Output	Address Chip select \overline{CS}		0.7	1 100 900	μs ns ns
t_{OD}	Output deselect				300	ns

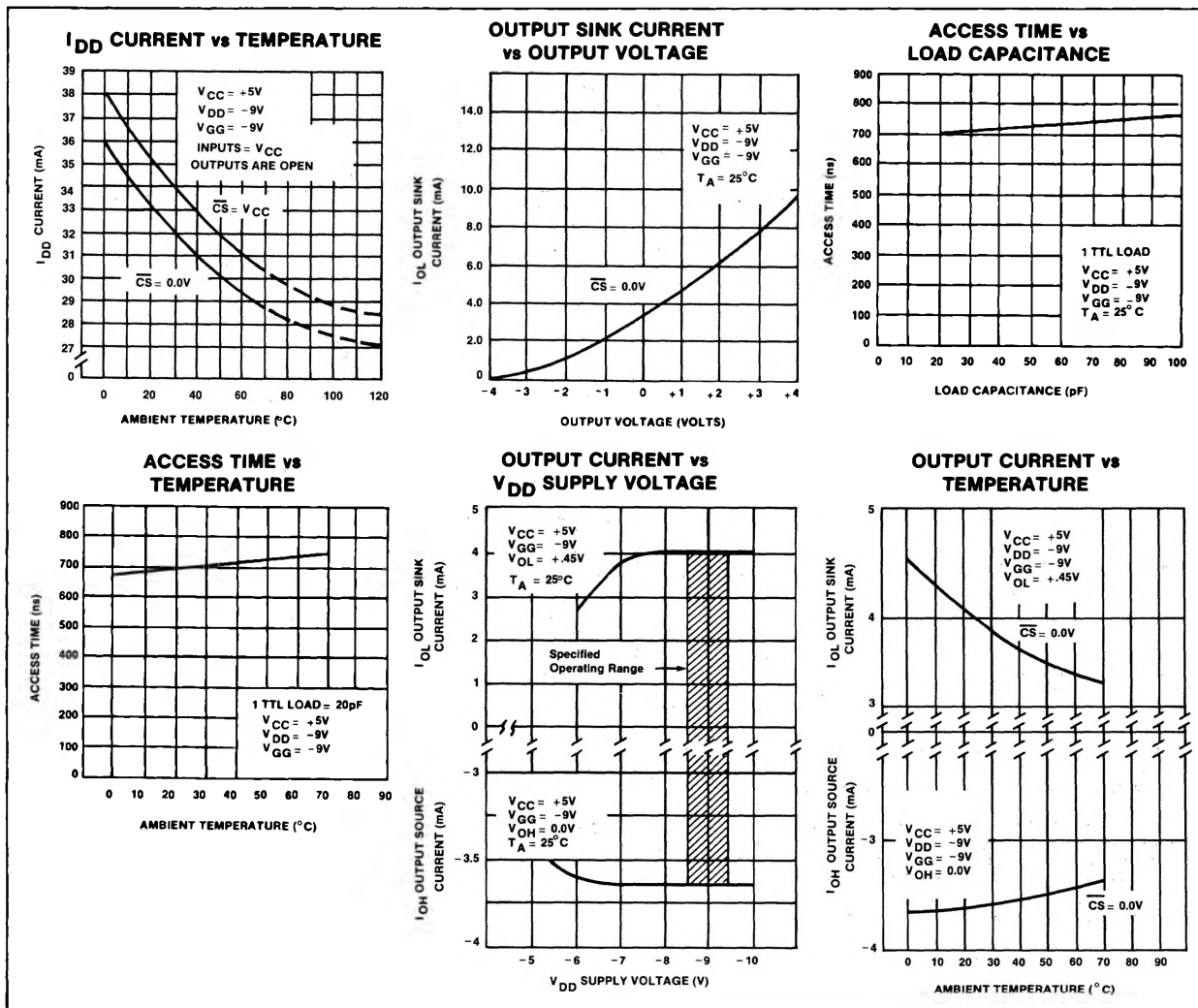
NOTES

- Signetics liability shall be limited to replacing any unit which fails to program as desired.
- The external lead connections to the 1702A differ depending on whether the device is being programmed or used in read mode. In the programming mode, the data inputs 1-8 are pins 4-11 respectively.
- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- Typical values are $T_A = 25^\circ\text{C}$ and at typical supply voltages.
- This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAMS



TYPICAL PERFORMANCE CHARACTERISTICS



DC AND OPERATING PROGRAMMING CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 0\text{V}$, $V_{BB} = +12\text{V} \pm 10\%$,
 $\overline{CS} = 0\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
V_{IHP}	Input voltage High		0.3		V
V_{IL1P}	Pulsed data low	-46	-48		
V_{IL2P}	Address low	-40	-48		
V_{IL3P}	Pulsed low V_{DD} and program	-46	-48		
V_{IL4P}	Pulsed low V_{GG}	-35	-40		
I_{LI1P}	Load current Address and data input	$V_{IN} = -48\text{V}$	10		mA
I_{LI2P}	Program and V_{GG}	$V_{IN} = -48\text{V}$	10		
I_{BB}	V_{BB} supply ¹		100		
I_{DDP}	Peak I_{DD} supply ²	$V_{DD} = V_{prog} = -48\text{V}$, $V_{GG} = -35\text{V}$	200	300	

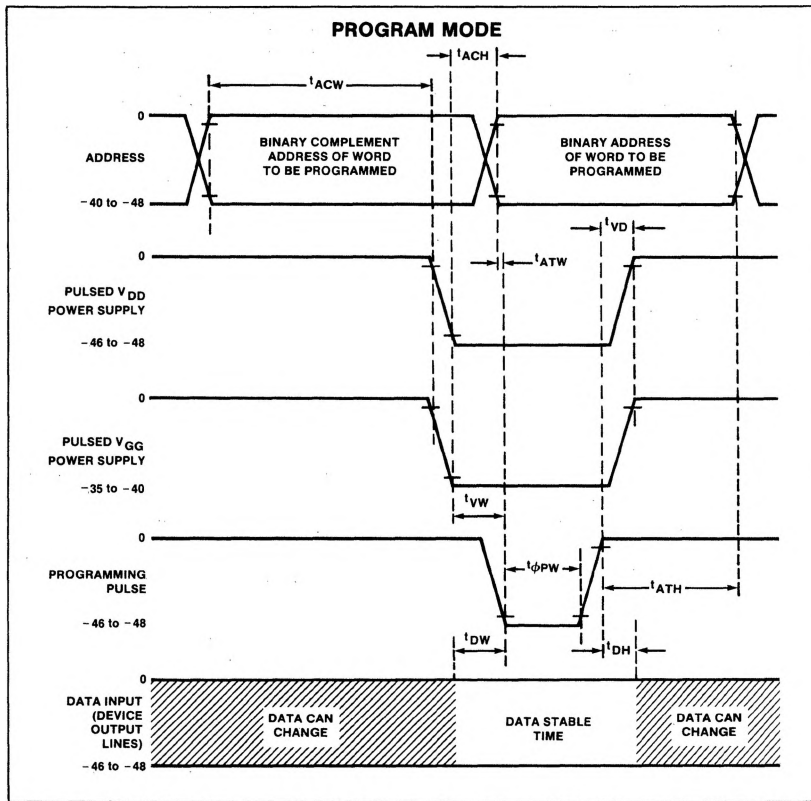
AC PROGRAMMING CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 0\text{V}$, $V_{BB} = +12\text{V} \pm 10\%$, $\overline{CS} = 0\text{V}$, unless otherwise specified,
 Input rise and fall times = $< 1\mu\text{s}$ unless otherwise specified.

PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
				Min	Typ	Max	
$t_{\theta PW}$	Duty cycle (V_{DD} , V_{GG}) Program pulse width		$V_{DD} = V_{prog} = -48\text{V}$, $V_{GG} = -35\text{V}$			20 3	% ms
t_{DW}	Setup and hold time Setup time	Programming pulse Data		25			μs
t_{DH}	Hold time	Data Programming pulse		10			
t_{VW}	Setup time	Programming pulse	Pulsed power supply	100			
t_{VD}	Hold time	Pulsed power supply	Programming pulse	10		100	
t_{ACW}	Setup time ³	Pulsed V_{DD} power supply	Address	25			
t_{ACH}	Hold time ³	Address Power supply	Pulsed V_{DD} power supply	25			
t_{ATW}	Setup time	Programming pulse Address	Address	10			
t_{ATH}	Hold time	Address Programming pulse	Programming pulse	10			

NOTES

- The V_{BB} supply must be limited to 100mA current to prevent damage to the device.
- I_{DDP} flows only during V_{DD} , V_{GG} on time. I_{DDP} should not be allowed to exceed 300mA for greater than 100 μs . Average power supply current I_{DDP} is typically 40mA at 20% duty cycle.
- All 8 address bits must be in the complement state when pulsed V_{DD} and V_{GG} move to their negative levels. The addresses (0-255) must be programmed as shown in the timing diagram.

TIMING DIAGRAM



OPERATION IN PROGRAM MODE

Initially, all 2048 bits of the ROM are in the low state. Information is introduced by selectively programming high's in the proper bit locations.

Word Address selection is done by the same decoding circuitry used in the Read mode (see dc Electrical Characteristics table). All 8 address bits must be in the binary complement state when pulsed V_{DD} and V_{GG} move to their negative levels. The addresses must be held in their binary complement state of a minimum of $25\mu\text{s}$ after V_{DD} and V_{GG} have moved to the negative levels. The addresses must then make the transition to their true state a minimum of $10\mu\text{s}$ before the program pulse is applied.

The 8 output terminals are used as data inputs to determine the information pattern in the 8 bits of each word. A low data input level (-48V) will then program a "1" and a high data input level (ground) will leave a "0" (see dc and Operating Programming Characteristics table). All 8 bits of one word are pro-

grammed simultaneously by setting the desired bit information patterns on the data input terminals.

During the programming, V_{GG} , V_{DD} and the program pulse are pulsed signals. We recommend the P+4P smart programming routine where P = the number of programming pulses for data to read true; P max = 256; and 4P = the number of over programming pulses applied.

ERASING PROCEDURE

The 1702A may be erased by exposure to high intensity short-wave ultraviolet light at a wavelength of 2537\AA . The recommended integrated dose (i.e., UV intensity x exposure time) is 6W-sec/cm^2 . Examples of ultraviolet sources which can erase the 1702A in 10 to 20 minutes are the Model UVS-54 and Model S-52 short-wave ultraviolet lamps manufactured by Ultra-Violet Products, Inc., 5114 Walnut Grove Avenue, San Gabriel, Ca. The lamps should be used without short-wave filters, and the 1702A to be erased should be placed about one inch away from the lamp tubes.