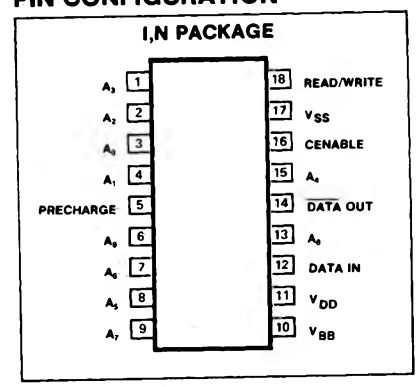
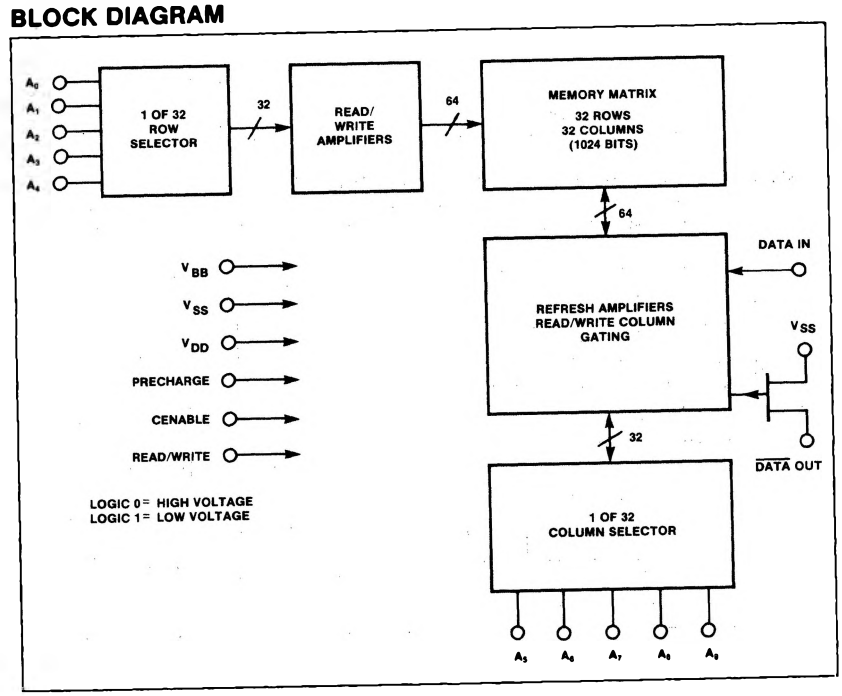
DESCRIPTION

The 1103 is designed for main memory applications where high performance, low cost and large bit storage are important design objectives. It is a random access memory element using enhancement mode p-channel MOS devices integrated on a monolithic array. It is fully decoded, permitting the use of an 18-pin dual in-line package. The dynamic circuitry dissipates significant power only during precharge. Information stored in the memory is non-destructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles and is required every 2ms. A separate cenable (chip enable) lead allows easy selection of an individual package when outputs are OR-tied. Use Signetics 8T25 sense amp, and 3207 clock driver.

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation	1	W
	All input or output voltages with respect to the most positive supply voltage, V_{BB}	-25 to 0.3	V
	Supply voltages V_{DD} and V_{SS} with respect to V_{BB}	-25 to 0.3	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{SS}[2] = 16V ± 5%, (V_{BB} - V_{SS})[3] = 3V to 4V, V_{DD} = 0V unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
	Low					
V_{IL1}[4]	All address and data in lines	T_A = 0°C	V_{SS} - 17		V_{SS} - 14.2	
V_{IL2}[4]	All address and data in lines	T_A = 70°C	V_{SS} - 17		V_{SS} - 14.5	
V_{IL3}[4,5]	Precharge, Cenable, Read/write inputs	T_A = 0°C	V_{SS} - 17		V_{SS} - 14.7	
V_{IL4}[4,5]	Precharge, Cenable, Read/write inputs	T_A = 70°C	V_{SS} - 17		V_{SS} - 15.0	
	High[4]					
V_{IH1}	All inputs	T_A = 0°C	V_{SS} - 1		V_{SS} + 1	
V_{IH2}	All inputs	T_A = 70°C	V_{SS} - 0.7		V_{SS} + 1	
	Output voltage	R_{LOAD} = 100Ω[6]				mV
V_{OL}	Low[7]					
	High					
V_{OH1}		T_A = 25°C	60	90	400	
V_{OH2}		T_A = 70°C	50	80	400	
	Supply current	T_A = 25°C, All addresses = 0V, Precharge = 0V				mA
I_{DD1}	During T_{PC}[8]	Cenable = V_{SS}		37	56	
I_{DD2}	During T_{OV}[8]	Cenable = 0V		38	59	
I_{DD3}	During T_{POV}[8]	Cenable = 0V		5.5	11	
I_{DD4}	During T_{CP}[8]	Cenable = V_{SS}		3	4	
I_{DDAV}	Average[9]	Cycle time = 580ns, Precharge width = 190ns		17	25	
I_{BB}	V_{BB} supply current				100	μA
	Output current	R_{LOAD} = 100Ω[6]				μA
	High					
I_{OH1}		T_A = 25°C	600	900	4000	
I_{OH2}		T_A = 70°C	500	800	4000	
	Capacitance[10]	f = 1MHz, All unused pins are at ac ground, V_{IN} = V_{SS}				pF
C_{AD}	Address				7	
C_{PR}	Precharge				18	
C_{CE}	Cenable				18	
C_{RW}	Read/write				15	
	Data input					
C_{IN1}		Cenable = 0V			5	
C_{IN2}		Cenable = V_{SS}			4	
	Data output					
C_{OUT}		V_{OUT} = 0V			3	

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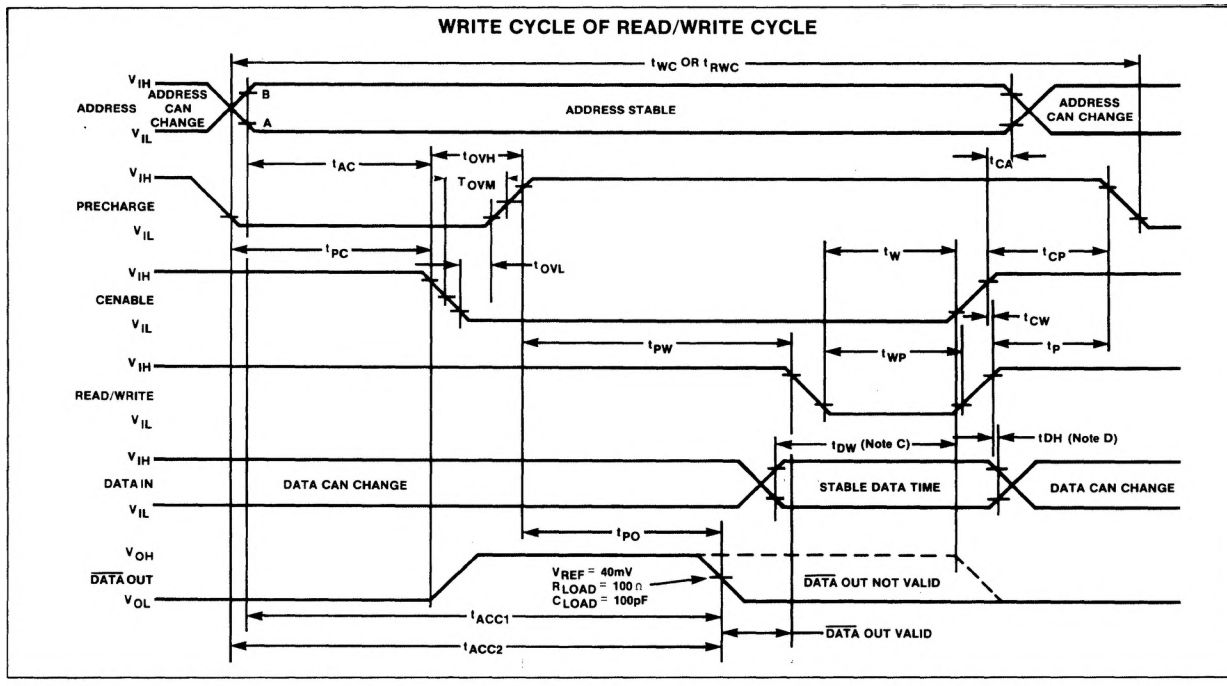
AC ELECTRICAL CHARACTERISTICS T_A = 0°C to 70°C, V_{SS} = 16 ± 5%, (V_{BB} – V_{SS}) = 3.0V to 4.0V, V_{DD} = 0V

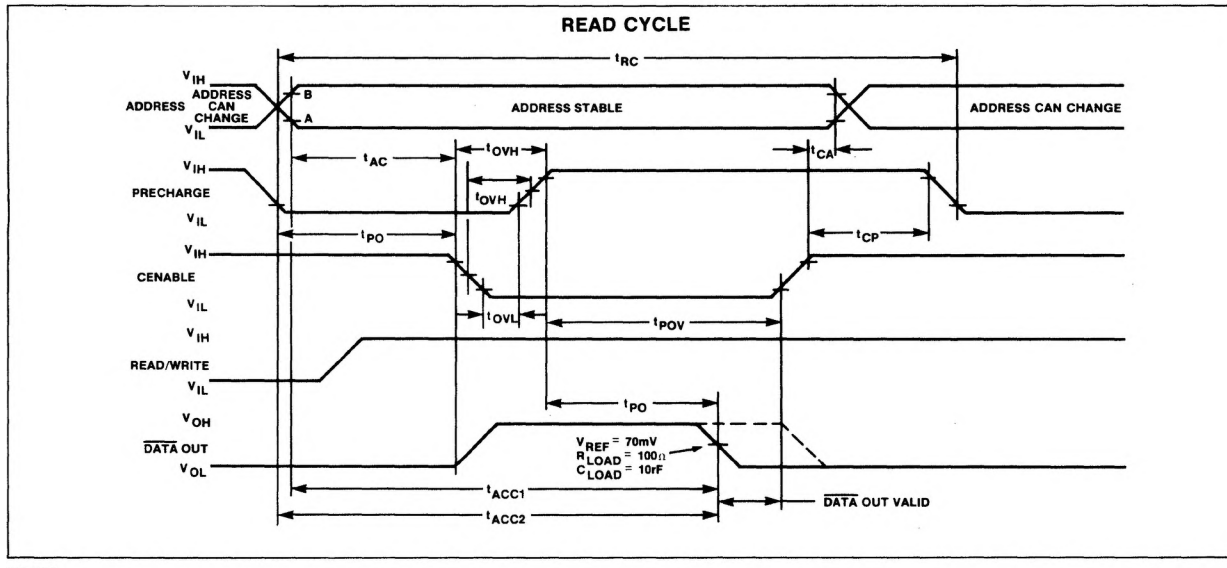
PARAMETER		TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
READ, WRITE AND READ/WRITE CYCLE								
T_{REF}	Time between refresh						2	ms
	Setup and hold time							ns
t_{AC}	Setup time[11]	Cenable	Address		115			
t_{CA}	Hold time	Address	Cenable		20			
	Delay time							ns
t_{PC}[11]		Cenable	Precharge		125			
t_{CP}		Precharge	Cenable		85			
	Precharge and cenable overlap			t = 20ns				ns
t_{OVL}	Low				25		75	
t_{OVH}	High						140	
t_{OVM}	50% points				45		95	
	READ CYCLE			$t_{AC(min)} + t_{OVL(min} + t_{PO(max)} =$ $2t, t_{PC(min)} + t_{OVL(min)} + t_{PO(max)}$ $+ 2t$, t = 20ns, C_{LOAD} = 100pF, R_{LOAD} = 100, V_{REF} = 40mV				
t_{RC}	Read cycle[11]				480			ns
	Delay time							ns
t_{POV}		End of cenable	Precharge		165		500	
t_{PO}		Output	End of precharge				120	
	Access time[11]							ns
t_{ACC1}		Output	Address		300			
t_{ACC2}		Output	Precharge		310			
WRITE OR READ/WRITE CYCLE				C_{LOAD} = 100pF, R_{LOAD} = 100, V_{REF} = 40mW				
t_{WC}	Write cycle[11]			t = 20ns	580			ns
t_{RWC}	Read/write cycle[11]			t = 20ns	580			ns
	Delay time							ns
t_{PW}		Read/write	Precharge		165		500	
t_{PO}		Output	End of precharge				120	
	Setup and hold time							ns
t_W	Setup time	Chip enable high	Read/write		80			
t_{DW}	Setup time	Chip enable high	Data		105			
t_{DH}	Hold time	Data	R/W high		10			
t_{CW}	Hold time	R/W high	Chip enable high				10	
t_{WP}	Read/write pulse width				50			ns
t_P	Time to next precharge				0			ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The V_{SS} current drain is equal to (I_{DD} + I_{OH}) or (I_{DD} + I_{OL}).
3. (V_{BB} – V_{SS}) supply should be applied at or before V_{SS}.
4. The maximum values for V_{IL} and the minimum values for V_{IH} are linearly related to temperature between 0°C and 70°C. Thus any value in between 0°C and 70°C can be calculated by using a straight-line relationship.
5. The maximum values for V_{IL} (for precharge, cenable and read/write) may be increased to V_{SS} – 14.2 at 0°C and V_{SS} – 14.5 at 70°C (same values as those specified for the address and data-in lines) with a 40ns degradation (worst case) in t_{AC}, t_{PC}, t_{RC}, t_{WC}, t_{RWC}, t_{ACC1} and t_{ACC2}.
6. This value of load resistance is used for measurement purposes. In applications the resistance may range from 100Ω to 1kΩ.
7. The output current when reading a low output is the leakage current of the 1103 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.
8. See Supply Current vs Temperature for guaranteed current at the temperature extremes. These values are taken from a single pulse measurement.
9. This parameter is periodically sampled and is not 100% tested.
10. This parameter is periodically sampled and is not 100% tested. It is measured at worst case operating conditions. Capacitance measurements for plastic package only.
11. These times will degrade by 40ns (worst case) if the maximum values for V_{IL} (for precharge, cenable and read/write inputs) go to V_{SS}– 14.2V at 0°C and V_{SS} – 14.5V at 70°C.

TIMING DIAGRAMS





NOTES

A. V_{DD} + 2V
B. V_{SS} - 2V
t_T is defined as the transitions between these two points.
C. t_{DW} is referenced to point 1 of the rising edge of cenable of read/write whichever occurs first.
D. t_{DH} is referenced to point 2 of the rising edge of cenable or read/write whichever occurs first.