signetics

4-BIT ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

10181

ADVANCE INFORMATION
TO BE ANNOUNCED

10181F: –30 to +85°C, CERDIP

DIGITAL 10,000 SERIES ECL

DESCRIPTION

The 10181 is an extremely versatile high speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic functions on two four-bit words. Using advanced circuit design techniques and double layer metalization the 10181 represents the state-of-the-art in standard ECL/LSI functions. As a result, the 10181 has the same power dissipation as the comparable TTL function, while increasing the speed of operation by a factor of 4.

The $\overline{M}$ input selects the arithemetic or logic mode of operation on 2 four-bit words. The desired arithmetic or logic function is selected by applying the appropriate binary word to the select inputs ($\overline{S0}$ thru $\overline{S3}$). Full internal carry is incorporated for ripple-through operation. Group carry propagate (P_G) and carry generate (G_G) are provided to allow fast addition of very long words using a second order look-ahead in conjunction with the 10179 full look-ahead carry block. The internal carry is enabled when the mode control input (M) has a low-level voltage applied (arithmetic operation). Full addition of two 32-bit words, with carry in and carry out can be performed in 18 ns. All inputs have 50kΩ internal pulldown resistors, and outputs are all open emitters for versatility in interconnect techniques.

FEATURES

- **FAST PROPAGATION DELAYS:**
  - **= 3.1 ns TYP ($\overline{C}_n$ TO $\overline{C}_{n+4}$)**
  - **= 5.0 ns TYP ($\overline{C}_n$ TO $\overline{F}_1$)**
  - **= 7.0 ns TYP ($\overline{A}1$, $\overline{B}1$ TO $\overline{F}1$)**
  - **= 5.0 ns TYP ($\overline{A}1$ TO $\overline{C}_{n+4}$)**
- **16 LOGIC OPERATIONS**
- **16 ARITHMETIC OPERATIONS**
- **POWER DISSIPATION = 600 mW/PACKAGE TYP (NO LOAD)**
- **HIGH Z INPUTS – INTERNAL 50 kΩ PULLDOWNS**
- **HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = –5.2 V ±5% RECOMMENDED**
- **OPEN EMITTERS FOR BUSSING AND LOGIC CAPABILITY**

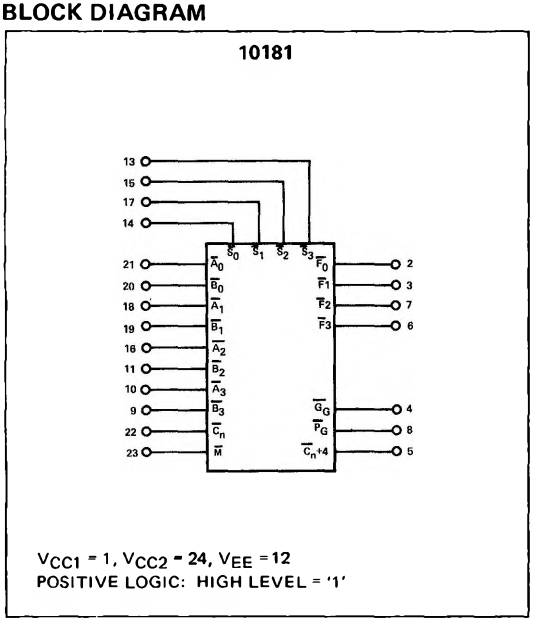
TEMPERATURE RANGE

- –30 to +85°C Operating Ambient

PACKAGE TYPE

- F: 24-Pin CERDIP

BLOCK DIAGRAM



V_{CC1} = 1, V_{CC2} = 24, V_{EE} = 12
POSITIVE LOGIC: HIGH LEVEL = '1'

FUNCTIONAL TRUTH TABLE

POSITIVE LOGIC

Function Select $\overline{S}3$	$\overline{S}2$	$\overline{S}1$	$\overline{S}0$	Logic Functions $\overline{M}$ is High $\overline{F}$	Arithmetic Operation $\overline{M}$ is Low $\overline{C}_n$ of LSB must be High $\overline{F}$*
L	L	L	L	$\overline{F} = A$	F = A minus 1
L	L	L	H	$\overline{F} = A + B$	F = A plus $(A + \overline{B})$
L	L	H	L	$\overline{F} = A + \overline{B}$	F = A plus (A + B)
L	L	H	H	$\overline{F}$ = Logical "1"	F = A times 2
L	H	L	L	$\overline{F} = A \cdot B$	F = (A · B) minus 1
L	H	L	H	$\overline{F} = B$	F = (A · B) plus $(A + \overline{B})$
L	H	H	L	$\overline{F} = A \circledcirc B$	F = A plus B
L	H	H	H	$\overline{F} = \overline{A} + B$	F = A plus (A · B)
H	L	L	L	$\overline{F} = A \cdot \overline{B}$	F = $(A \cdot \overline{B})$ minus 1
H	L	L	H	$\overline{F} = A \oplus B$	F = A minus B minus 1
H	L	H	L	$\overline{F} = \overline{B}$	F = $(A \cdot \overline{B})$ plus (A + B)
H	L	H	H	$\overline{F} = \overline{A} + \overline{B}$	F = $(A \cdot \overline{B})$ plus A
H	H	L	L	$\overline{F}$ = Logical "0"	F = minus 1 (two's complement)
H	H	L	H	$\overline{F} = \overline{A} \cdot B$	F = $(A + \overline{B})$ plus 0
H	H	H	L	$\overline{F} = \overline{A} \cdot \overline{B}$	F = (A + B) plus 0
H	H	H	H	$\overline{F} = \overline{A}$	F = A plus 0

*$\overline{F}$ outputs of ALU are one's complement of function listed below.

ELECTRICAL CHARACTERISTICS
(at Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	10181 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	Gnd
Power Supply Drain Current	I_E	12	–	–	–	–	145	–	–	mAdc	–	–	–	–	12	1,24
Input Current	I_{inH}	9	–	–	–	–	245	–	–	µAdc	9	–	–	–	12	1,24
		10	–	–	–	–	220	–	–		10	–	–	–		
		11	–	–	–	–	245	–	–		11	–	–	–		
		13	–	–	–	–	200	–	–		13	–	–	–		
		14	–	–	–	–	265	–	–		14	–	–	–		
		15	–	–	–	–	265	–	–		15	–	–	–		
		16	–	–	–	–	220	–	–		16	–	–	–		
		17	–	–	–	–	265	–	–		17	–	–	–		
		18	–	–	–	–	220	–	–		18	–	–	–		
		19	–	–	–	–	245	–	–		19	–	–	–		
		20	–	–	–	–	245	–	–		20	–	–	–		
		21	–	–	–	–	220	–	–		21	–	–	–		
		22	–	–	–	–	290	–	–		22	–	–	–		
		23	–	–	–	–	200	–	–		23	–	–	–		
Input Leakage Current	I_{inL}	9	–	–	0.5	–	–	–	–	µAdc	–	9	–	–	12	1,24
		10	–	–							–	10	–	–		
		11	–	–							–	11	–	–		
		13	–	–							–	13	–	–		
		14	–	–							–	14	–	–		
		15	–	–							–	15	–	–		
		16	–	–							–	16	–	–		
		17	–	–							–	17	–	–		
		18	–	–							–	18	–	–		
		19	–	–							–	19	–	–		
		20	–	–							–	20	–	–		
		21	–	–							–	21	–	–		
		22	–	–							–	22	–	–		
		23	–	–							–	23	–	–		
High Output Voltage	V_{OH}	*	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	*	*	–	–	12	1,24
Low Output Voltage	V_{OL}	*	−2.000	−1.675	−1.990	–	−1.650	−1.920	−1.615	Vdc	*	*	–	–	12	1,24
High Threshold Voltage	V_{OHA}	*	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	**	**	12	1,24
Low Threshold Voltage	V_{OLA}	*	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	**	**	12	1,24

*Test all input-output combinations according to Function Table.
**For threshold level test, apply threshold input level to only one input pin at a time.

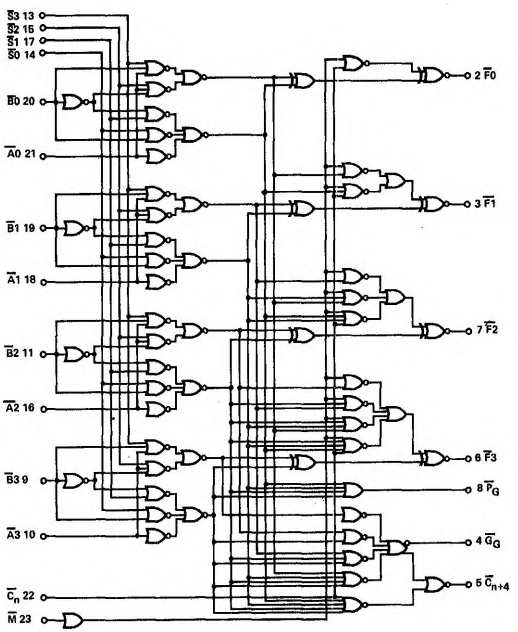
Each ECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

Characteristic	Symbol	Input	Output	Conditions†	AC Switching Characteristics +25°C Min	Typ	Max	Unit
Propagation Delay	t + +	$\overline{C_n}$	$\overline{C_{n+4}}$	–	–	3.1	–	ns
	t − −				–	3.1	–	
Rise Time	t +				–	2.0	–	
Fall Time	t −				–	2.0	–	
Propagation Delay	t + +	$\overline{C_n}$	F1	$\overline{M}$ is Low	–	4.9	–	ns
	t + −				–	5.0	–	
	t − +				–	4.9	–	
	t − −				–	5.0	–	
Rise Time	t +				–	2.0	–	
Fall Time	t −				–	2.0	–	
Propagation Delay	t + +	$\overline{A1}$	$\overline{F1}$	–	–	7.0	–	ns
	t + −				–	7.0	–	
	t − +				–	7.0	–	
	t − −				–	7.0	–	
Rise Time	t +				–	2.0	–	
Fall Time	t −				–	2.0	–	
Propagation Delay	t + +	A1	P_G	–	–	3.0	–	ns
	t − −				–	3.0	–	
Rise Time	t +				–	2.0	–	
Fall Time	t −				–	2.0	–	
Propagation Delay	t + +	$\overline{A1}$	$\overline{G_G}$	–	–	4.0	–	ns
	t − −				–	5.0	–	
Rise Time	t +				–	2.0	–	
Fall Time	t −				–	2.0	–	
Propagation Delay	t + −	$\overline{A1}$	$\overline{C_{n+4}}$	–	–	5.4	–	ns
	t − +				–	4.4	–	
Rise Time	t +				–	2.0	–	
Fall Time	t −				–	2.0	–	
Propagation Delay	t + +	$\overline{B1}$	$\overline{F1}$	$\overline{S1}$ and $\overline{S2}$ High, $\overline{S0}$ or $\overline{S3}$ Low	–	7.0	–	ns
	t + −				–	7.0	–	
	t − +				–	7.0	–	
	t − −				–	7.0	–	
Rise Time	t +				–	2.0	–	
Fall Time	t −				–	2.0	–	

Characteristic	Symbol	Input	Output	Conditions†	AC Switching Characteristics +25°C Min	Typ	Max	Unit
Propagation Delay	t + +	$\overline{B1}$	$\overline{P_G}$	$\overline{S0}$ Low, $\overline{S1}$ High	–	3.0	–	ns
	t − −				–	3.0	–	
Rise Time	t +				–	2.0	–	
Fall Time	t −				–	2.0	–	
Propagation Delay	t + +	$\overline{B1}$	$\overline{G_G}$	$\overline{S2}$ High, $\overline{S3}$ Low	–	4.0	–	ns
	t − −				–	5.0	–	
Rise Time	t +				–	2.0	–	
Fall Time	t −				–	2.0	–	
Propagation Delay	t + −	$\overline{B1}$	$\overline{C_{n+4}}$	$\overline{S1}$ and $\overline{S2}$ High, $\overline{S0}$ or $\overline{S3}$ Low	–	5.4	–	ns
	t − +				–	4.4	–	
Rise Time	t +				–	2.0	–	
Fall Time	t −				–	2.0	–	
Propagation Delay	t + +	$\overline{B1}$	F1	S1 or S2 Low	–	7.5	–	ns
	t + −				–	8.0	–	
	t − +				–	7.5	–	
	t − −				–	8.0	–	
Rise Time	t +				–	2.0	–	
Fall Time	t −				–	2.0	–	
Propagation Delay	t + −	$\overline{B1}$	$\overline{P_G}$	$\overline{S1}$ Low	–	4	–	ns
	t − +				–	4	–	
Rise Time	t +				–	2.0	–	
Fall Time	t −				–	2.0	–	
Propagation Delay	t − +	$\overline{B1}$	$\overline{G_G}$	$\overline{S2}$ Low	–	5.2	–	ns
	t + −				–	5.7	–	
Rise Time	t +				–	2.0	–	
Fall Time	t −				–	2.0	–	
Propagation Delay	t + −	$\overline{B1}$	$\overline{C_{n+4}}$	$\overline{S0}$ or $\overline{S1}$ or $\overline{S2}$ or $\overline{S3}$ Low	–	6.9	–	ns
	t − +				–	6.6	–	
Rise Time	t +				–	2.0	–	
Fall Time	t −				–	2.0	–	

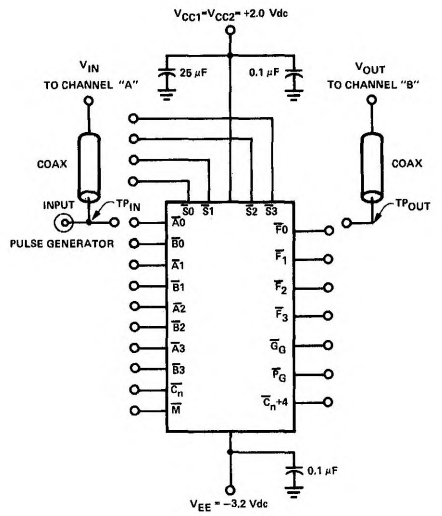
†High = +1.11 V
Low = +0.31 V
$V_{CC1} = V_{CC2} = +2.0$ Vdc = −3.2 Vdc, $V_{EE} = -3.2$ Vdc

LOGIC DIAGRAM



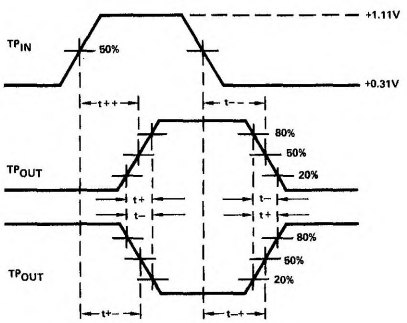
Positive logic: High Level = "1"

SWITCHING TIME TEST CIRCUIT



INPUT PULSE
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

PROPAGATION DELAY WAVEFORM @ 25°C



All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <1/4 inch from TP_{in} to input pin and TP_{out} to output pin.