10139-F,N

DESCRIPTION

The 10139 is organized as an array of 32 words and 8 bits. The initial unprogrammed state is 0 (low). The user may program 1's to obtain any desired pattern. Outputs go to the 0 (low) state when the chip enable input is high, allowing wired-OR output connections. A 50Ω output drive capability makes the part suitable for use in high performance ECL systems.

FEATURES

- **Access time: 15ns typ**
- **Power dissipation: 580mW typ**
- **Field programmable (Ni-Cr link)**
- **Fully decoded**
- **High impedance inputs (50kΩ pulldown)**
- **Open emitter outputs (50Ω drive)**
- **Fully compatible with Signetics ECL 10K products**

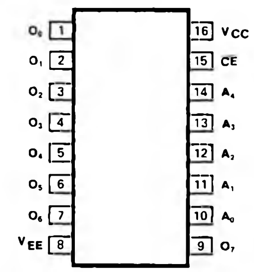
APPLICATIONS

- **Programmable logic**
- **Control stores**
- **Microprogramming**
- **Hardwired algorithms**

RECOMMENDED OPERATING VOLTAGE

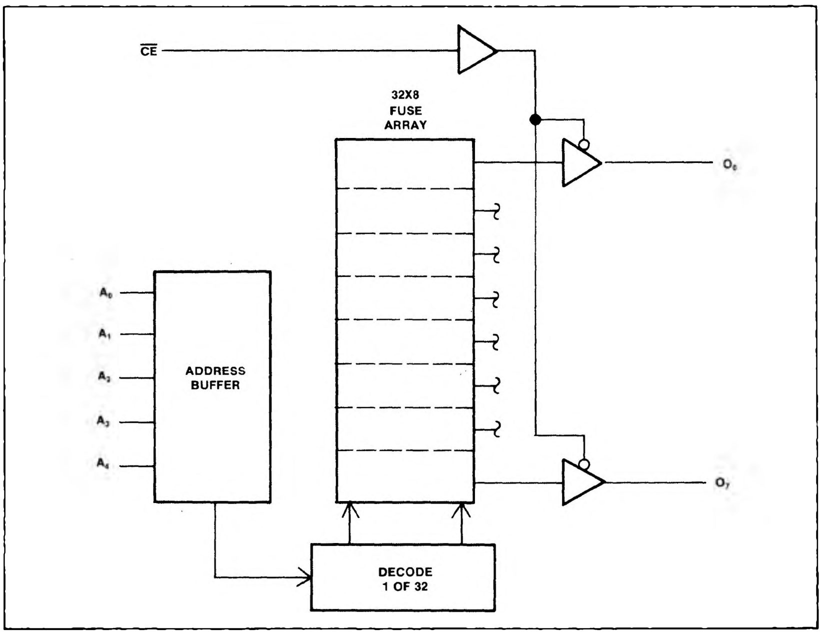
- **V_{CC} = GND, V_{EE} = -5.2V ± 5%**

PIN CONFIGURATION



*F = Cerdip
N = Plastic

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
T_A	Temperature range Operating	-30 to +85	°C

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DC ELECTRICAL CHARACTERISTICS V_{CC} = 0V, V_{EE} = -5.2V, R_L = 50Ω to -2V, Vdc ± 1%

PARAMETER		TEST CONDITIONS	-30°C			+25°C			+85°C			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Input voltage											V
V_{IL}	Low		-1.890			-1.850			-1.825			
V_{IH}	High				-0.890			-0.810			-0.700	
V_{ILA}	Low threshold				-1.500			-1.475			-1.440	
V_{IHA}	High threshold		-1.205			-1.105			-1.035			
	Output voltage											V
V_{OL}	Low	V_{IH} = Max, V_{IL} = Min	-1.89		-1.675	-1.85	-1.70	-1.65	-1.825		-1.615	
V_{OH}	High		-1.06		-0.89	-0.96	-0.89	-0.81	-0.89		-0.70	
V_{OLA}	Low threshold	V_{IHA} = Min, V_{ILA} = Max			-1.655			-1.63			-1.595	
V_{OHA}	High threshold		-1.08			-0.98			-0.91			
	Input current											µA
I_{IL}	Low	V_{IL} = Min				0.5						
I_{IH}	High	V_{IH} = Max						265				
I_{EE}	Power supply drain current						110	145				mA

AC ELECTRICAL CHARACTERISTICS V_{CC} = 2V, R_L = 50Ω to ground, -30°C ≤ T_A ≤ 85°C, V_{EE} = -3.2V

PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
	Access time						ns
T_{AA}		Output	Address		15	22	
T_{CE}		Output	Chip enable		10	17	
	Disable time						ns
T_{CD}		Output	Chip disable		10	17	
	Rise and fall time						ns
t_+	Rise time (20-80%)				4.0		
t_-	Fall time (20-80%)				4.0		

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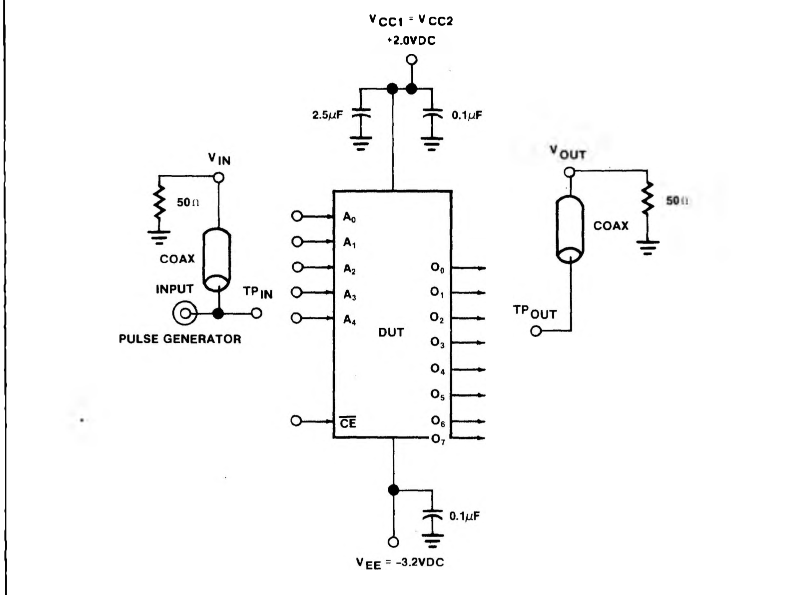
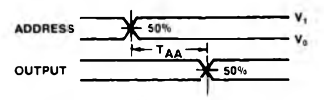
TEST LOAD CIRCUIT



Input pulse: $t_+ = t_- = 2.0 - 0.2ns$ (20 to 80%)

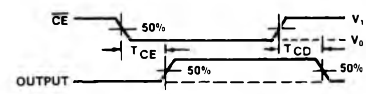
VOLTAGE WAVEFORMS

ADDRESS ACCESS TIME



Input pulse conditions: $V_0 = 0.31V$, $V_1 = 1.11V$, $t_r = 2ns$ (20 to 80%), $t_f = 2ns$ (20 to 80%)

CHIP ENABLE/DISABLE TIMES



Input pulse conditions: $V_0 = 0.31V$, $V_1 = 1.11V$, $t_r = 2ns$ (20 to 80%), $t_f = 2ns$ (20 to 80%)

NOTES

1. Dc and ac specifications apply after thermal equilibrium has been established, with transverse air flow greater than 500 linear ft/min.
2. For ac tests, all input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be < 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50Ω termination to ground is located in each scope input. Unused outputs are connected to a 50Ω resistor to ground.
3. Test procedures are shown for only 1 input or set of input conditions. Other inputs are tested in the same manner.

PROGRAMMING SYSTEMS SPECIFICATIONS

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Power supply voltage					V
V_{CCP}	To program		11.5	12.0	12.5	
V_{CCV}	To verify		5.0	5.2	5.4	
I_{CCP}	Programming supply current	$V_{CC} = 12.0V$			250	mA
	Address voltage					V
V_{IH}	High		4.0		4.6	
V_{IL}	Low		0		1.0	
	Max time at $V_{CC} = V_{CCP}$				1.0	sec
I_{OP}	Output programming current		3.75	4.25	4.75	mA
t_p	Output program pulse width		0.5		1.0	ms
	Output pulse rise time				10	μs
	Programming pulse delay*					ms
t_d	Following V_{CC} change		0.1		1.0	
t_{d1}	Between output pulses		0.01		1.0	

*Maximum is specified to minimize the amount of time V_{CC} is at 12V.

PROGRAMMING PROCEDURE

The 10139 is shipped with all bits at logical low. To program logical high's, proceed as follows:

1. Connect a 7.5kΩ resistor from each output to ground. This prevents crosstalk into unselected outputs during programming.
2. Connect pin 8 (V_{EE}) to ground and pin 16 (V_{CC}) to +5.2V.
3. Address the desired word location using 0 to 1.0V for a logic low and 4.0 to 4.6V for a logic high.
4. Raise V_{CC} to 12V. Wait 100μs (min) for settling. Maximum time at 12V is 1.0 sec.
5. Apply a +4.25mA current pulse to the first output to be programmed. Output pin voltage will be approximately 1.2V above V_{CC}, and the 7.5kΩ resistor will take 1.75mA. Pulse duration is 0.5 to 1.0ms. Other outputs may be programmed sequentially using a delay of .01 to 1.0ms between current pulses.
6. Return V_{CC} to 5.2V and verify the word. Repeat step 5 once only if any bit failed to program.
7. Repeat steps 3, 4, 5 and 6 for all address locations to be programmed.
8. Verify complete truth table.

TYPICAL FUSING PATH