

10132F: -30 TO +85°C, CERDIP

DIGITAL 10,000 SERIES ECL

DESCRIPTION

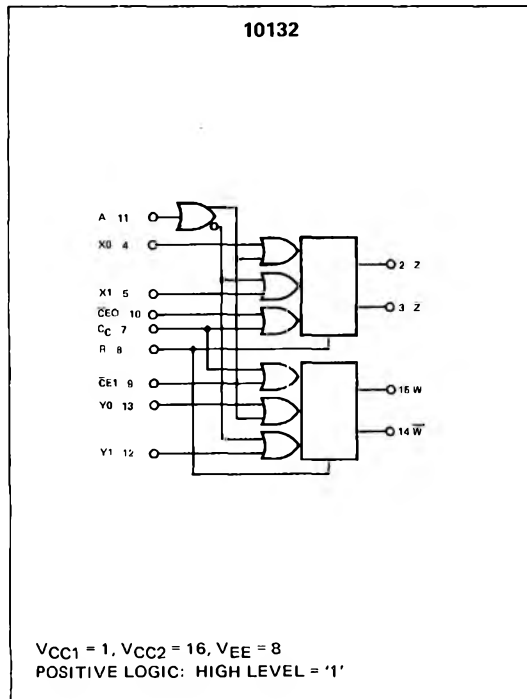
The 10132 is a dual clocked D-type latch with 2 to 1 data multiplexing. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable (\overline{CE}) inputs must be in the low state. In this state, the enable inputs perform the function of enabling the common clock, (C_C).

Any change at the selected D input will be reflected at the output while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data or select inputs will not affect the output information.

The asynchronous reset input (R) overrides the clock inputs.

Input pull-down resistors eliminate the need to tie unused inputs to V_{EE} .

LOGIC DIAGRAM



FEATURES

- HIGH SPEED COMBINED MULTIPLEXER - LATCH IMPROVES SYSTEM PERFORMANCE.
- MULTIPLEXED INPUTS TO REDUCE PACKAGE COUNT
- FAST PROPAGATION DELAY = 2.5 ns TYP (DATA) = 3.7 ns TYP (SELECT) = 3.0 ns TYP (RESET) = 4.0 ns TYP (CLOCK)
- LOW POWER DISSIPATION = 200 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY - CAN DRIVE 50 Ω LINES
- HIGH Z INPUTS - INTERNAL 50 k Ω PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: $V_{EE} = -5.2 V \pm 5\%$ RECOMMENDED
- OPEN EMITTER LOGIC AND BUSSING CAPABILITY

APPLICATIONS

- COMBINED MULTIPLEXER - REGISTER FOR:
 - high speed central processors
 - high speed peripherals
 - high speed minicomputers
 - high speed accumulators
 - communication systems

TRUTH TABLE

| R | X_{in} | C_C | \overline{CE} | Z_{n+1} |
|---|----------|-------|-----------------|-----------|
| L | L | L | L | L |
| L | L | L | H | Z_n |
| L | L | H | L | Z_n |
| L | L | H | H | Z_n |
| L | H | L | L | H |
| L | H | L | H | Z_n |
| L | H | H | L | Z_n |
| L | H | H | H | Z_n |
| H | ϕ | H | ϕ | L |

ϕ = Don't Care.

$$X_{in} = \overline{A} \cdot X0 + A \cdot X1$$

TEMPERATURE RANGE

- -30 to +85°C Operating Ambient

PACKAGE TYPE

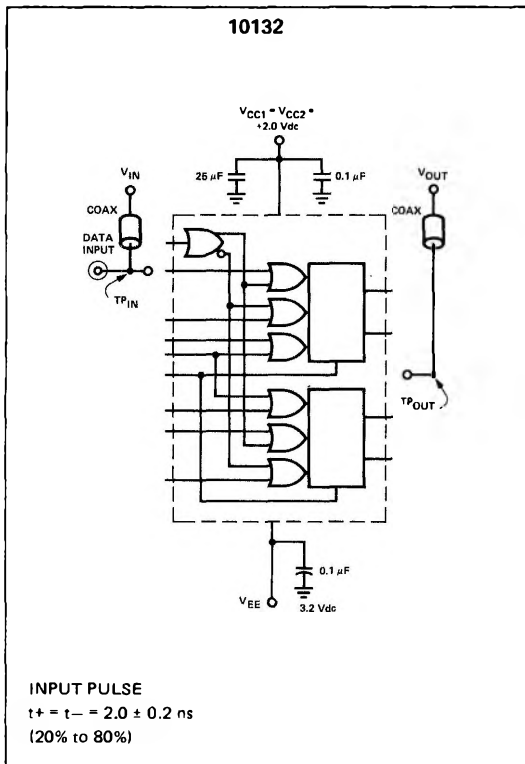
- F: 16-Pin CERDIP

ELECTRICAL CHARACTERISTICS
(at Listed Voltages and Ambient Temperatures).

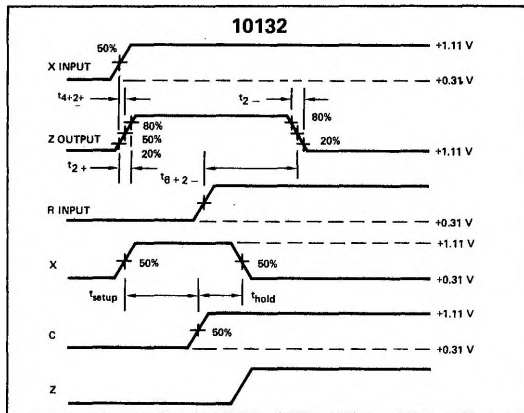
| Characteristic | Symbol | Pin Under Test | 10132 Test Limits | | | | | | | | | | TEST VOLTAGE VALUES | | | | | Gnd | |
|---|-------------------|--------------------|-------------------|--------|--------|------|--------|--------|--------|-----|-----------------|-----------------|---------------------|----------|-----------|--------|--------|------|------|
| | | | -30°C | | | | | +25°C | | | | | +85°C | | | | | | |
| | | | Min | Max | Min | Typ | Max | Min | Max | Min | Max | Min | Max | Min | Max | VEE | | | |
| Power Supply Current | I _E | 8 | 50 | | | | | | | | | | mA _{dc} | 7.11 | - | | | 8 | 1.10 |
| Input Current | I _{in} H | 4 | 290 | | | | | | | | | | μA _{dc} | 4 | - | | | 8 | 1.16 |
| | | 5 | 290 | | | | | | | | | | | 6,11 | - | | | 8 | 1.16 |
| | | 6 | 390 | | | | | | | | | | | 6,7 | - | | | 8 | 1.16 |
| | | 7 | 290 | | | | | | | | | | | 7 | - | | | 8 | 1.16 |
| | | 10 | 220 | | | | | | | | | | | 10 | - | | | 8 | 1.16 |
| | | 11 | 220 | | | | | | | | | | | 11 | - | | | 8 | 1.16 |
| Logic "1" Output Voltage | V _{OH} | 2 | -1.060 | -0.890 | -0.980 | - | -0.810 | -0.890 | -0.700 | - | - | V _{dc} | 4 | 7.9,10 | - | - | 8 | 1.16 | |
| | | 2 | -1.060 | -0.890 | -0.980 | - | -0.810 | -0.890 | -0.700 | - | - | V _{dc} | 6,11 | 7.9,10 | - | - | 8 | 1.16 | |
| Logic "0" Output Voltage | V _{OL} | 3 | -1.890 | -1.676 | -1.860 | - | -1.660 | -1.826 | -1.615 | - | - | V _{dc} | 4 | 7.9,11 | - | - | 8 | 1.16 | |
| | | 3 | -1.890 | -1.676 | -1.860 | - | -1.660 | -1.826 | -1.615 | - | - | V _{dc} | 6,11 | 7.9,10 | - | - | 8 | 1.16 | |
| Logic "1" Threshold Voltage | V _{OHA} | 2 | -1.080 | - | -0.980 | - | - | -0.910 | - | - | V _{dc} | - | 7.9,10 | 4 | - | - | 8 | 1.16 | |
| | | 2 | -1.080 | - | -0.980 | - | - | -0.910 | - | - | V _{dc} | 11 | 7.9,10 | 5 | - | - | 8 | 1.16 | |
| Logic "0" Threshold Voltage | V _{OLA} | 3 | - | -1.658 | - | - | -1.630 | - | -1.595 | - | V _{dc} | - | 7.9,10 | 4 | - | - | 8 | 1.16 | |
| | | 3 | - | -1.655 | - | - | -1.630 | - | -1.595 | - | V _{dc} | 11 | 7.9,10 | 5 | - | - | 8 | 1.16 | |
| Switching Times (50-ohm load) (See Figure 1) | | | | | | | | | | | | +1.11 V | +0.31 V | Pulse In | Pulse Out | -3.2 V | +2.0 V | | |
| Propagation Delay | Data | t ₄₊₂₊ | 2 | - | - | 2.5 | - | - | - | - | ns | - | 7.9,10 | 4 | 2 | 8 | 1.16 | | |
| | Reset | t ₆₊₂₋ | 2 | - | - | 3.0 | - | - | - | - | ns | 7 | - | 6 | - | 8 | 1.16 | | |
| | Clock | t ₇₋₂₊ | 2 | - | - | 4.0 | - | - | - | - | ns | 4 | - | 7 | - | 8 | 1.16 | | |
| | Select | t ₁₁₊₂₊ | 2 | - | - | 3.7 | - | - | - | - | ns | 5 | 7 | 11 | - | 8 | 1.16 | | |
| Setup Time | Data | t _{setup} | 2 | - | - | 1.6 | - | - | - | - | ns | - | 11 | 4,10 | 2 | 8 | 1.16 | | |
| | Select | t _{setup} | 2 | - | - | 2.6 | - | - | - | - | ns | 5 | 7 | 10,11 | 2 | 8 | 1.16 | | |
| Hold Time | Data | t _{hold} | 2 | - | - | 0.0 | - | - | - | - | ns | - | 11 | 4,10 | 2 | 8 | 1.16 | | |
| | Select | t _{hold} | 2 | - | - | -0.6 | - | - | - | - | ns | 8 | 7 | 10,11 | 2 | 8 | 1.16 | | |
| Rise Time (20% to 80%) | | t ₂₊ | 2 | - | - | 2.0 | - | - | - | - | ns | - | 7.9,10 | 4 | 2 | 8 | 1.16 | | |
| Fall Time (20% to 80%) | | t ₂₋ | 2 | - | - | 2.0 | - | - | - | - | ns | - | 7.9,10 | 4 | 2 | 8 | 1.16 | | |

*All other inputs tested in the same manner.

SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

- Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to -2.0 volts.
- For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to Input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
- Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
- All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.