DESCRIPTION

The 10130 is a clocked dual D-type latch. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{C}_E$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock ($\overline{C}$).

Any change at the D input will be reflected at the output while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

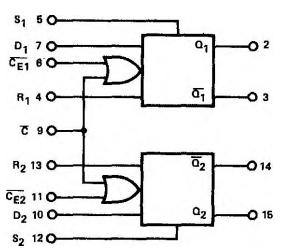
Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

The asynchronous set (S) and reset (R) inputs are effective only with the clock input high.

The 10130 is pin compatible with the 10131 dual master/slave type D flip-flop.

LOGIC DIAGRAM

10130



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = "1"

FEATURES

- FAST PROPAGATION DELAY = 2.5 ns TYP (DATA)
  = 2.8 ns TYP (SET, RESET)
  = 3.0 ns TYP (CLOCK)
- LOW POWER DISSIPATION = 140 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY – CAN DRIVE 50Ω LINES
- HIGH Z INPUTS – INTERNAL 50 kΩ PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = −5.2 V ±5% RECOMMENDED
- OPEN EMITTER LOGIC AND BUSSING CAPABILITY
- PIN COMPATIBLE WITH 10131

APPLICATIONS

- HIGH SPEED REGISTERS
- CONTROL LATCHES
- STATUS LATCHES

TRUTH TABLE

D	C	S	R	Q_{n+1}
L	L	ϕ	ϕ	I
A	I	ϕ	ϕ	H
ϕ	H	L	L	Q_n
ϕ	H	H	L	H
ϕ	H	L	H	L
ϕ	H	H	H	N.D.

$C = \overline{CE} + \overline{C}$
ϕ = Don't care
N.D. = Not defined

TEMPERATURE RANGE

- −30 to +85°C Operating Ambient

PACKAGE TYPE

- F: 16-Pin CERDIP

ELECTRICAL CHARACTERISTICS
(at Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.600	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

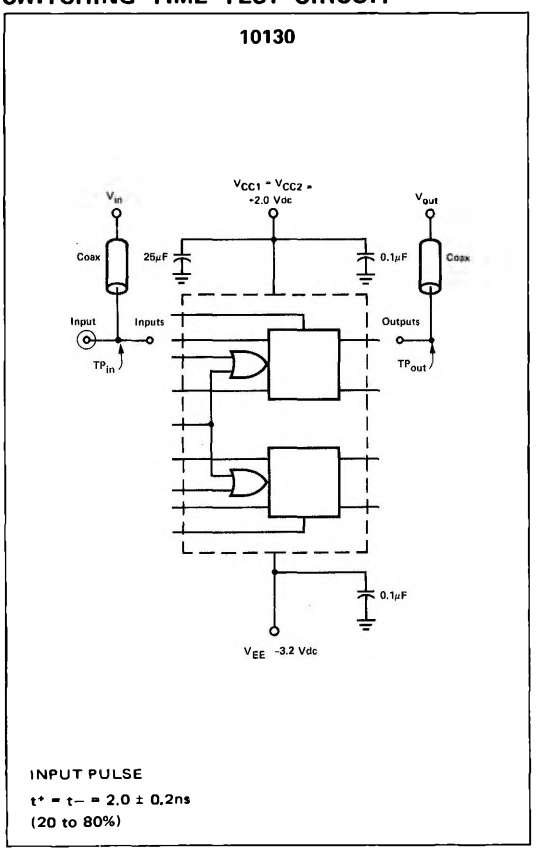
Characteristic	Symbol	Pin Under Test	10130 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	28	35	–	–	mAdc	9	–	–	–	8	1,16
Input Current	I_{inH}	6,11	–	–	–	–	220	–	–	μAdc	6	–	–	–	8	1,16
		9	–	–	–	–	265	–	–		4,9	–	–	–		
		4,5,7	–	–	–	–	286	–	–		5,9	–	–	–		
	I_{inL}	4*	–	–	0.50	–	–	–	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	7	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	7	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	0.910	–	Vdc	7	–	–	9	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	7	–	9	8	1,16
Switching Times (50 Ω load) (See Figure 1)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{7-2-}	2	–	–	1.5	2.5	4.3	–	–	ns	–	–	7	2	8	1,16
	t_{7+2+}		–	–	1.5	2.5	4.3	–	–		–	–	7			
	t_{5+2+}		–	–	1.5	2.8	4.3	–	–		6	–	5			
	t_{4+2-}		–	–	1.2	2.8	4.3	–	–		6	–	4			
Rise Time (20% to 80%)	t_{2+}		–	–	1.1	2.5	4.5	–	–		–	–	7			
Fall Time (20% to 80%)	t_{2-}		–	–	1.1	2.5	4.5	–	–		–	–	7			
Setup Time	t_{setup}†	2	–	–	–	–	2.5	–	–	ns	–	–	6,7	2	8	1,16
Hold Time	t_{hold}††	2	–	–	1.5	–	–	–	–	ns	–	–	6,7	2	8	1,16

*All other inputs are tested in the same manner.

† t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).

††t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

SWITCHING TIME TEST CIRCUIT

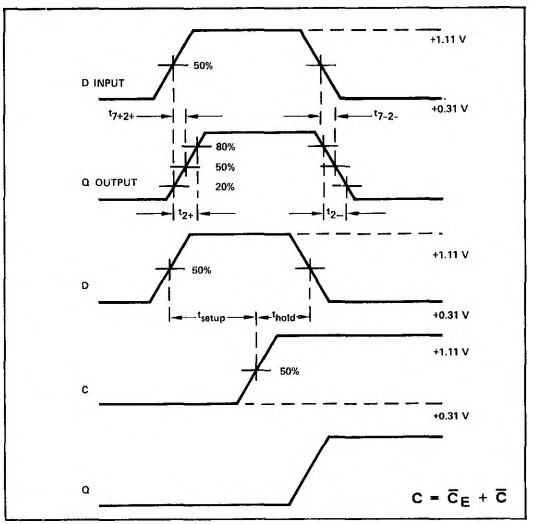


INPUT PULSE

$t^+ = t^- = 2.0 \pm 0.2$ns

(20 to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C

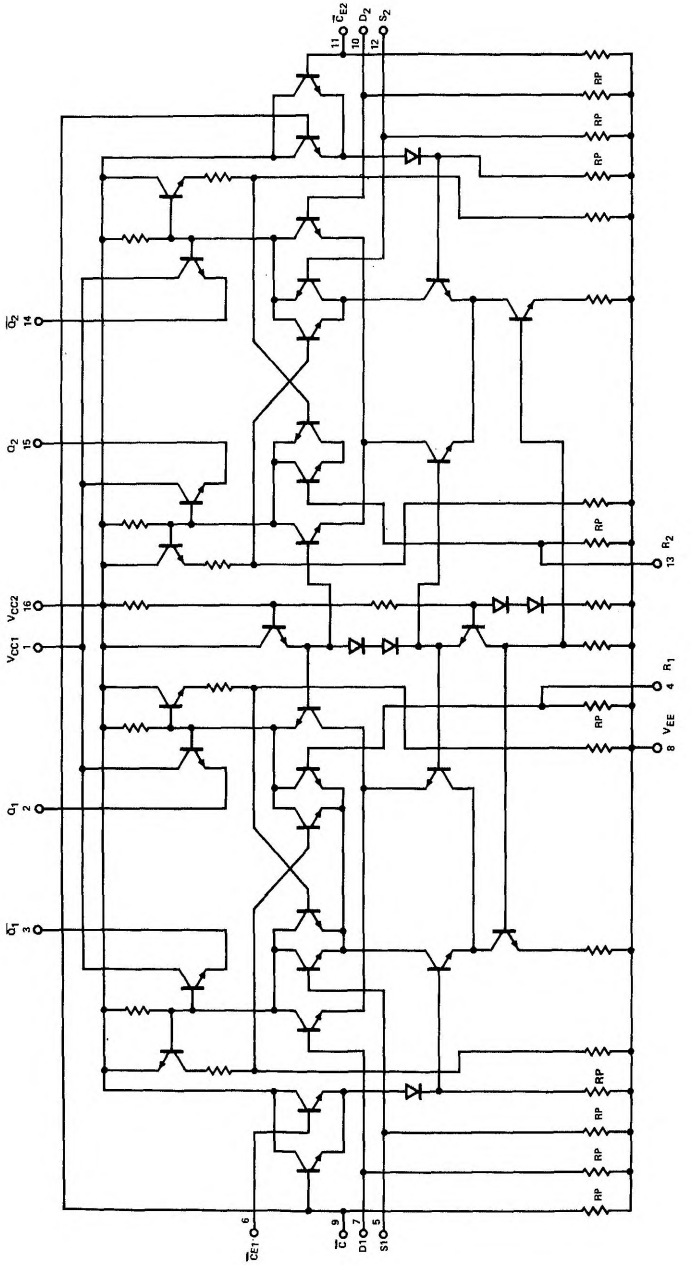


NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

CIRCUIT SCHEMATIC

10130



$C = \overline{C}_E + \overline{C}$. All Rp = 50 kΩ.

signetics

DUAL D-TYPE MASTER-SLAVE FLIP-FLOP 10131

10131F: –30 to +85°C

DIGITAL 10,000 SERIES ECL

DESCRIPTION

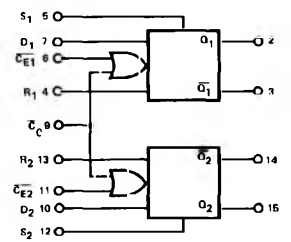
The 10131 is a dual master-slave type D flip-flop. Asynchronous set (S) and reset (R) override clock ($\overline{C}$) and clock enable ($\overline{CE}$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the clock enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master-slave construction. Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}. Output rise and fall times have been optimized to provide relaxation of system design and layout criteria.

The 10131 is pin compatible with the 10130 dual D-type latch.

LOGIC DIAGRAM

10131



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = "1"

FEATURES

- f_{TOG} = 125 MHz MIN
  = 160 MHz TYP
- FAST PROPAGATION DELAY
  = 2.8 ns TYP (SET, RESET)
  = 3.0 ns TYP (CLOCK)
- LOW POWER DISSIPATION = 235 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY
  – CAN DRIVE 50 Ω LINES
- HIGH Z INPUTS – INTERNAL 50 kΩ PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = –5.2 V ±5% RECOMMENDED
- OPEN EMITTER LOGIC AND BUSSING CAPABILITY
- PIN COMPATIBLE WITH 10130

APPLICATIONS

- CONTROL LOGIC
- STATUS LOGIC
- COUNTERS
- SHIFT REGISTER
- PRESCALERS

TRUTH TABLE

D	C*	S	R	Q_{n+1}
ϕ	L	L	L	Q_n
L	H	L	L	L
H	H	L	L	H
ϕ	*ϕ	H	L	H
ϕ	ϕ	L	H	L
ϕ	ϕ	H	H	N.D.

*An H represents a transition from L to H between t = n and t = n + 1

$C = C_C + \overline{CE}$

N.D. = Not defined

TEMPERATURE RANGE

- –30 to +85°C Operating Ambient

PACKAGE TYPE

- F: 16-Pin CERDIP