DESCRIPTION

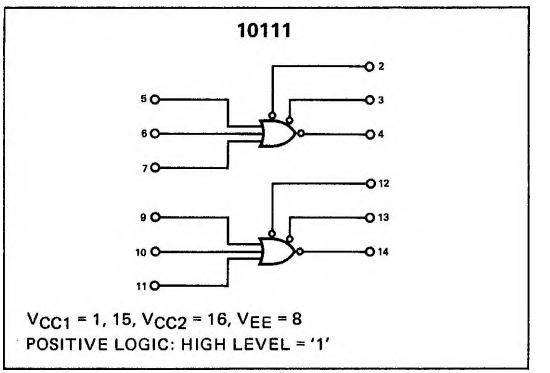
The 10111 is a dual high speed 3-input 3-output NOR gate. The 10111 is designed to drive up to three transmission lines simultaneously. The multiple outputs of this device also allow the wire-"OR"-ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines from a single point makes the 10111 particularly useful in clock distribution applications where minimum clock skew is desired.

FEATURES

- **FAST PROPAGATION DELAY = 2.4 ns TYP (ALL OUTPUTS LOADED)**
- **POWER DISSIPATION = 150 mW/PACKAGE TYP (NO LOAD)**
- **VERY HIGH FANOUT CAPABILITY – CAN DRIVE SIX 50 Ω LINES**
- **HIGH Z INPUTS – INTERNAL 50 kΩ PULLDOWNS**
- **HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = –5.2 V ±5% RECOMMENDED**
- **OPEN EMITTERS FOR BUSSING AND LOGIC CAPABILITY**

LOGIC DIAGRAM



V_{CC1} = 1, 15, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = '1'

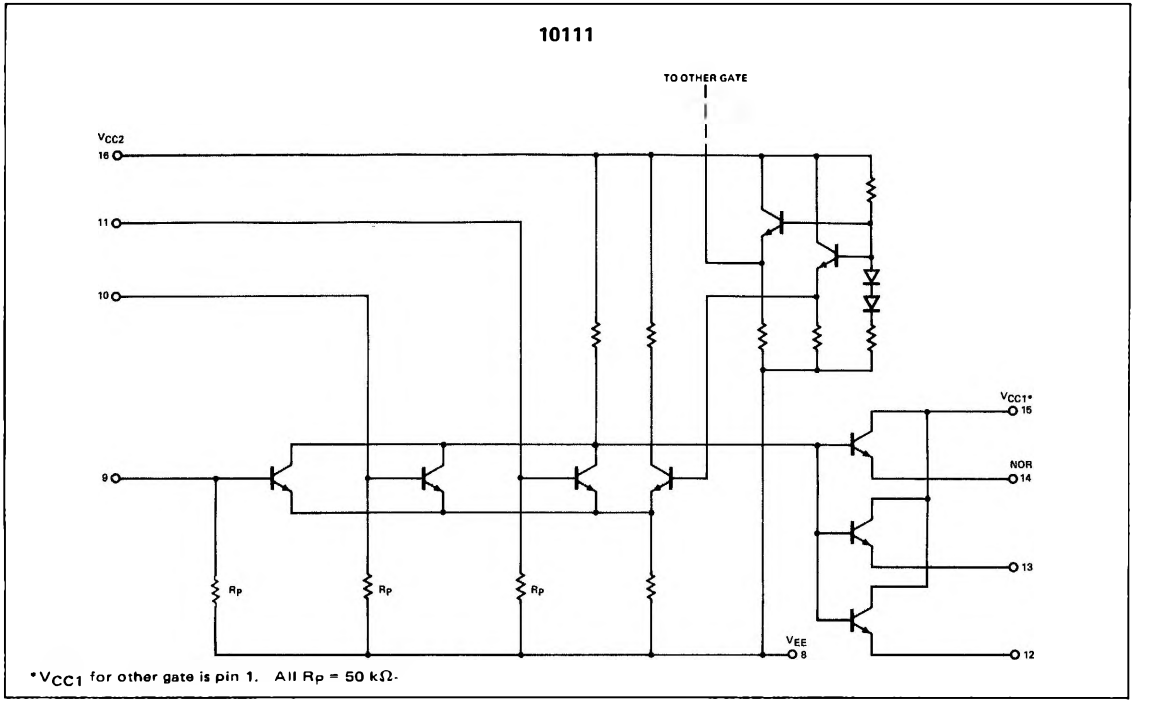
TEMPERATURE RANGE

- –30 to +85°C Operating Ambient

PACKAGE TYPE

B: 16-Pin Silicone DIP
F: 16-Pin CERDIP

CIRCUIT SCHEMATIC



*V_{CC1} for other gate is pin 1. All Rp = 50 kΩ.

ELECTRICAL CHARACTERISTICS

(at Listed Voltages and Ambient Temperatures).

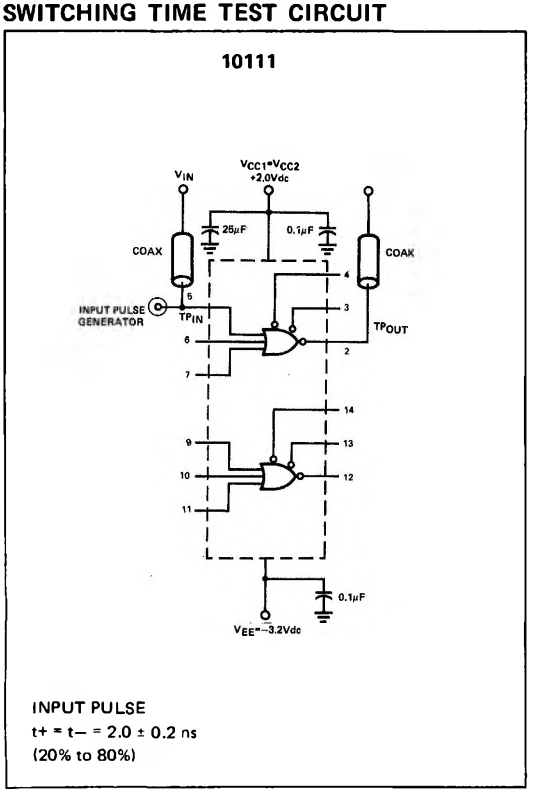
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	10111 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	–	38	–	–	mAdc	–	–	–	–	8	1,15,16
	I_{inH}	5,6,7	–	–	–	–	435	–	–	μAdc	*	–	–	–	8	1,15,16
	I_{inL}	5,6,7	–	–	0.5	–	–	–	–	μAdc	–	*	–	–	8	1,15,16
Logic "1" Output Voltage	V_{OH}	2	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	–	5	–	–	8	1,15,16
		3	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	–	6	–	–	8	1,15,16
		4	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	–	7	–	–	8	1,15,16
Logic "0" Output Voltage	V_{OL}	2	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	5	–	–	–	8	1,15,16
		3	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	6	–	–	–	8	1,15,16
		4	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	7	–	–	–	8	1,15,16
Logic "1" Threshold Voltage	V_{OHA}	2	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	–	5	8	1,15,16
		3	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	–	6	8	1,15,16
		4	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	–	7	8	1,15,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	5	–	8	1,15,16
		3	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	6	–	8	1,15,16
		4	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	7	–	8	1,15,16
Switching Times ** (50-ohm load)													Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	$t_{5+\ 2-}$	2	1.4	3.5	1.4	2.4	3.5	1.5	3.8	ns	–	–	5	2	8	1,15,16
	$t_{5-\ 2+}$	2									–	–		2		
	$t_{5+\ 3-}$	3									–	–		3		
	$t_{5-\ 3+}$	3									–	–		3		
	$t_{5+\ 4-}$	4									–	–		4		
	$t_{5-\ 4+}$	4									–	–		4		
Rise Time (20% to 80%)	t_{2+}	2	1.0		1.1	2.2	3.5	1.2	3.8		–	–		2		
	t_{3+}	3									–	–		3		
	t_{4+}	4									–	–		4		
Fall Time (20% to 80%)	t_{2-}	2									–	–		2		
	t_{3-}	3									–	–		3		
	t_{4-}	4									–	–		4		

*Individually test each input using the pin connections shown.

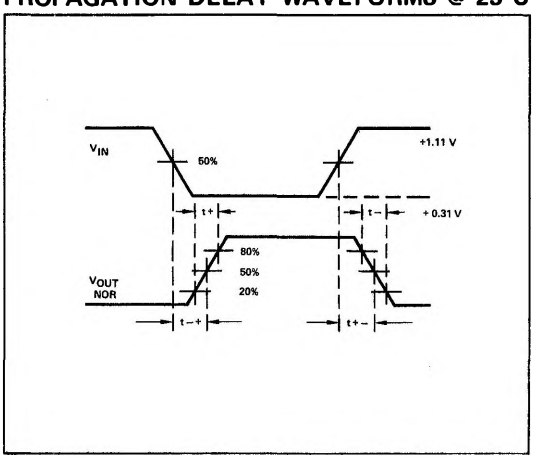
**Unused outputs connected to a 50-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT



INPUT PULSE
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 5 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.