DESCRIPTION

The 10105 package contains one 3 input OR/NOR gate, and two 2 input OR/NOR gates. The 10105 is optimized for high performance logic applications. Each gate has an excellent speed power product of 50 picojoules. All inputs are terminated with a 50 kΩ resistor to V_{EE} which eliminates the need to tie unused inputs low. The high impedance inputs and high output fanout is ideal for a transmission line environment. This gate meets the ECL 10,000 Series standard voltage, current, and rise and fall time specifications.

Complementary outputs make the 10105 particularly useful for differential line driving.

FEATURES

- **FAST PROPAGATION DELAY = 2.0 ns TYP**
- **POWER DISSIPATION = 75 mW/PACKAGE TYP (NO LOAD)**
- **VERY HIGH FANOUT CAPABILITY — CAN DRIVE 50 Ω LINES**
- **HIGH Z INPUTS — INTERNAL 50 kΩ PULLDOWNS**
- **HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = −5.2 V ±5% RECOMMENDED**
- **COMPLEMENTARY OR/NOR OUTPUTS**
- **OPEN EMITTER LOGIC AND BUSSING CAPABILITY**

TEMPERATURE RANGE

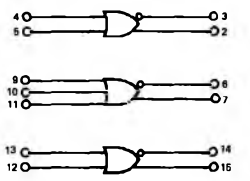
- −30 to +85°C Operating Ambient

PACKAGE TYPE

B: 16-Pin Silicone DIP
F: 16-Pin CERDIP

LOGIC DIAGRAM

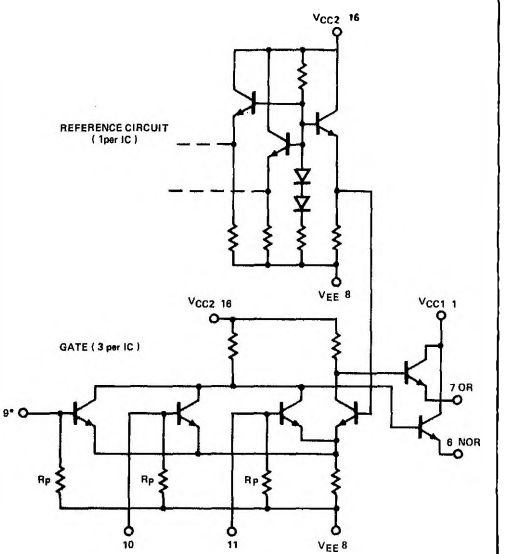
10105



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = '1'

CIRCUIT SCHEMATIC

10105



All R_P = 50 kΩ
*3rd input on one gate only.

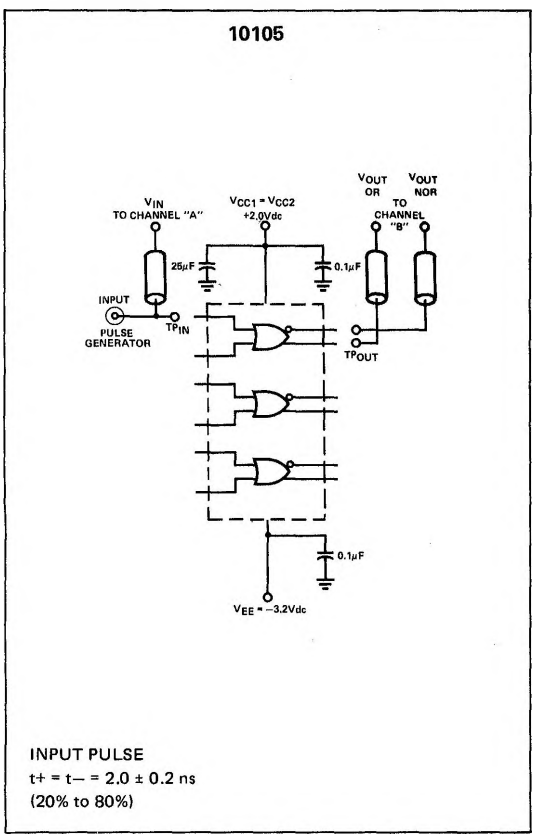
ELECTRICAL CHARACTERISTICS
(at Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	10105 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	16	21	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	–	–	–	266	–	–	μAdc	4	–	–	–	8	1,16
	I_{inL}	4	–	–	0.5	–	–	–	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	3	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	–	4	–	–	8	1,16
		2	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	4	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	4	–	–	–	8	1,16
		2	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	–	4	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	3	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	–	4	8	1,16
		2	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	4	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	4	–	8	1,16
		2	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	–	4	8	1,16
Switching Times * (50-ohm load)													Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	t_{4+3-}	3	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	–	–	4	3	8	1,16
	t_{4-3+}	3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	3	↓	↓
	t_{4+2+}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	6	↓	↓
	t_{4-2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	6	↓	↓
Rise Time (20% to 80%)	t_{3+}	3	1.1	3.6	1.1	↓	3.3	1.1	3.7	↓	–	–	↓	3	↓	↓
	t_{2+}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	6	↓	↓
Fall Time (20% to 80%)	t_{3-}	3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	3	↓	↓
	t_{2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	6	↓	↓

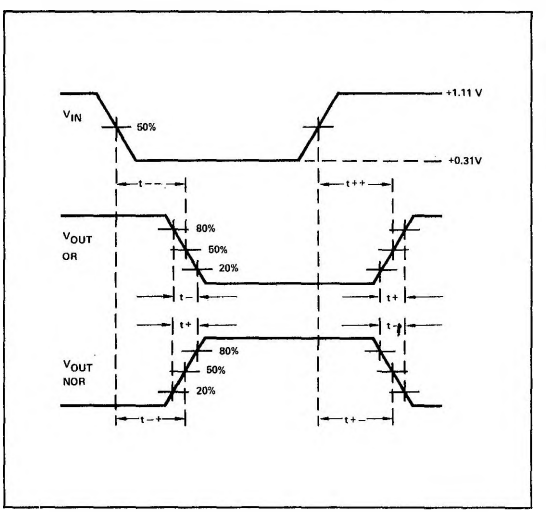
*Unused outputs connected to a 50-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT



INPUT PULSE
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:
1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 3 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.