ADVANCED INFORMATION

DESCRIPTION

The 10100 is a high speed Quad 3-Input NOR Gate. All inputs are terminated with a 50K ohm resistor to V_{EE} which eliminates the need to tie unused inputs low. The gate has an excellent speed-power product of 50 picojoules. The 10100 is optimized for high performance logic applications. This gate meets the ECL 10,000 Series standard voltage current and rise and fall time specifications.

FEATURES

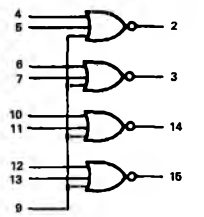
- FAST PROPAGATION DELAY = 2.0ns TYPICAL
- LOW POWER DISSIPATION = 100mW/PACKAGE – (NO LOAD)
- HIGH FANOUT CAPABILITY
  - CAN DRIVE FOUR 50 OHM LINES
  - DC OUTPUT LOADING FACTOR OF 90X4
- HIGH Z INPUTS – DC LOADING FACTOR OF 1
- INTERNAL 50K OHM PULLDOWN RESISTORS
- OUTPUT RISE AND FALL TIMES
  - 3.5ns TYPICAL (10% TO 90%)
  - 2.0ns TYPICAL (20% TO 80%)
- SEPARATE OUTPUT EMITTER FOLLOWER V_{CC} PIN – NEGLIGIBLE COUPLING
- HIGH NOISE IMMUNITY/NOISE GENERATION RATIO
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = 5.2V ± 5% RECOMMENDED
- MINIMUM CHANGE IN SYSTEM CHARACTERISTICS OCCURS WITHIN ± 10% V_{EE}
- OPEN EMITTER LOGIC AND BUSSING CAPABILITY

ELECTRICAL CHARACTERISTICS

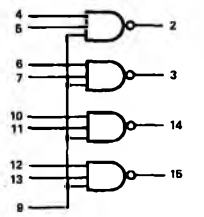
Conditions:	T_A = 25°C, V_{EE} = −5.2V ± 1%
1. I_E	= 20mA dc typical = 26mA dc max.
2. I_{inH}	= 265μA dc max. = 550μA dc max. (Pin 9)
Conditions:	T_A = 25°C, V_{CC} = +2.0V ± 1%, V_{EE} = −3.2V ± 1%, 50 ohm loads
3. t_{pd}	= 2.0ns typical (t+−, t−+)
4. t_r, t_f	= 2.0ns typical (20% to 80%)

LOGIC DIAGRAM

10100



Positive Logic: High Level = '1'



Negative Logic: Low Level = '1'

V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8

TEMPERATURE RANGE

- −30 to +85° C Operating Ambient

RECOMMENDED OPERATING VOLTAGE

- V_{CC1} = V_{CC2} = GND, V_{EE} = 5.2V ± 5%

PACKAGE TYPES

- B: 16 pin Silicone Dip
- F: 16 pin Cerdip