100315 Low-Skew Quad Clock Driver

Check for Samples: 100315

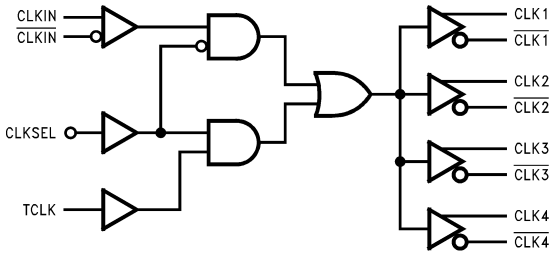
FEATURES

- **Low output to output skew (≤50 ps)**
- **Differential inputs and outputs**
- **Secondary clock available for system level testing**
- **2000V ESD protection**
- **Voltage compensated operating range: −4.2V to −5.7V**
- **Standard Microcircuit Drawing**
  - **(SMD) 5962-9469601**

DESCRIPTION

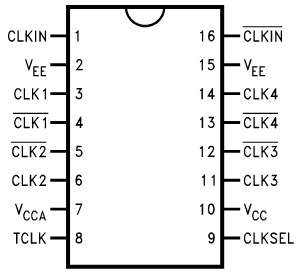
The 100315 contains four low skew differential drivers, designed for generation of multiple, minimum skew differential clocks from a single differential input. This device also has the capability to select a secondary single-ended clock source for use in lower frequency system level testing. The 100315 is a 300 Series redesign of the 100115 clock driver.

Logic Diagram



Connection Diagram

Figure 1. Flatpak



Pin Names	Description
CLKIN, $\overline{\text{CLKIN}}$	Differential Clock Inputs
$CLK_{1–4}$, $\overline{CLK}_{1–4}$	Differential Clock Outputs
TCLK	Test Clock Input (1)
CLKSEL	Clock Input Select (1)

(1) TCLK and CLKSEL are single-ended inputs, with internal 50 kΩ pulldown resistors.

Truth Table(1)

CLKSEL	CLKIN	$\overline{CLKIN}$	TCLK	CLK_N	$\overline{CLK_N}$
L	L	H	X	L	H
L	H	L	X	H	L
H	X	X	L	L	H
H	X	X	H	H	L

(1) L = Low Voltage Level
H = High Voltage Level
X = Don't Care

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Above which the useful life may be impaired	
Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Case Temperature under Bias (T_C)	–55°C to +125°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{CC} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V
ESD (2)	≥2000V

(1) Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.
(2) ESD testing conforms to MIL-STD-883, Method 3015.

Recommended OperatingConditions

Case Temperature (T_C)	
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Military Version
DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND [1]

Symbol	Parameter	Min	Typ	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025		−870	mV	0°C to +125°C	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V	*(2) (3) (1)
		−1085		−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830		−1620	mV	0°C to +125°C			
		−1830		−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035			mV	0°C to +125°C	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 50Ω to −2.0V	(2) (3) (1)
		−1085			mV	−55°C			
V_{OLC}	Output LOW Voltage			−1610	mV	0°C to +125°C			
				−1555	mV	−55°C			

(1) Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.
(2) F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides “cold start” specs which can be considered a worst case condition at cold temperatures.
(3) Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND (1)

Symbol	Parameter	Min	Typ	Max	Units	T_C	Conditions	Notes
V_{DIFF}	Input Voltage Differential	150			mV	−55°C to +125°C	Required for Full Output Swing	∗(2) (3) (1)
V_{CM}	Common Mode Voltage	V_{CC} − 2.0		V_{CC} − 0.5	V	−55°C to +125°C		(2) (3) (1)
V_{IH}	Single-Ended Input High Voltage	−1165		−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs	(2) (3) (1) (4)
V_{IL}	Single-Ended Input Low Voltage	−1830		−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs	(2) (3) (1) (4)
I_{IH}	Input HIGH Current CLKIN, $\overline{CLKIN}$			150	µA	−55°C to +125°C	V_{IN} = $V_{IH(Max)}$	(2) (3) (1)
	TCLK			450	µA			
	CLKSEL			380	µA			
I_{CBO}	Input Leakage Current	−10			µA	−55°C to +125°C	V_{IN} = V_{EE}	(2) (3) (1)
I_{EE}	Power Supply Current, Normal	−80		−25	mA	−55°C to +125°C		(2) (3) (1)

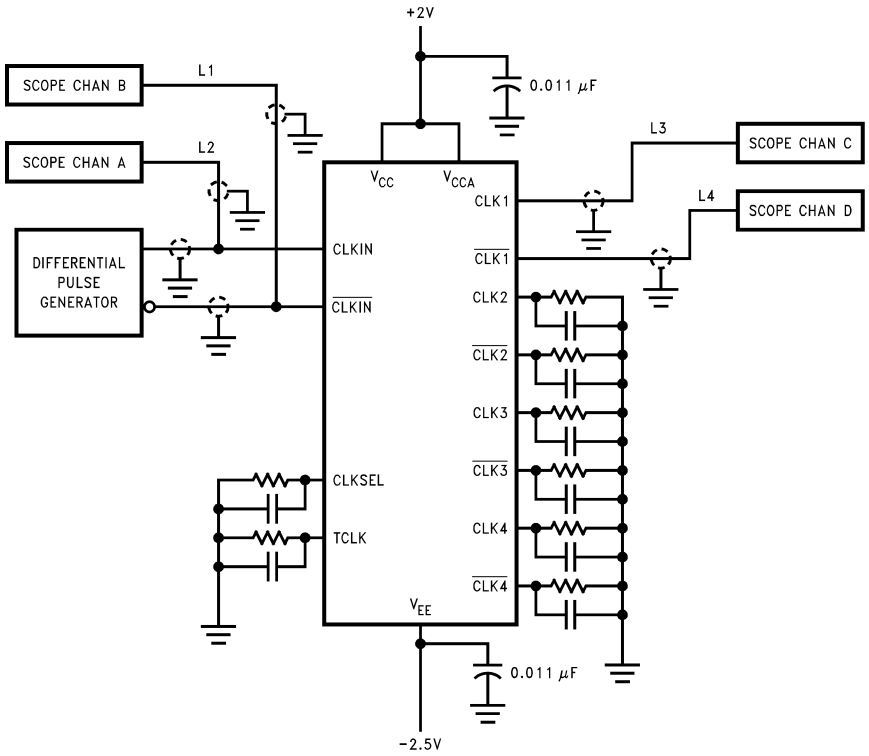
(1) Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.
(2) F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides “cold start” specs which can be considered a worst case condition at cold temperatures.
(3) Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.
(4) Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH}, t_{PHL}	Propagation Delay $\overline{CLKIN}$, CLKIN to $CLK_{(1–4)}$, $\overline{CLK}_{(1–4)}$	0.58	0.88	0.63	0.88	0.72	1.02	ns	Figure 2 Figure 3	*(1) (2) (3)
t_{PLH}, t_{PHL}	Propagation Delay, TCLK to $CLK_{(1–4)}$, $\overline{CLK}_{(1–4)}$	0.30	1.60	0.30	1.50	0.40	1.70	ns		
$t_{S\ G–G}$	Skew Gate to Gate (4)		120		100		120	ps		(3)
t_{TLH}, t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	0.90	0.25	0.85	0.20	0.85	ns		

(1) F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C, then testing immediately after power-up. This provides “cold start” specs which can be considered a worst case condition at cold temperatures.
(2) Screen tested 100% on each device at +25°C temperature only, Subgroup A9.
(3) Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.
(4) Maximum output skew for any one device.



Shown for testing CLKIN to CLK1 in the differential mode.

L1, L2, L3 and L4 = equal length 50Ω impedance lines.

All unused inputs and outputs are loaded with 50Ω in parallel with ≤3 pF to GND.

Scope should have 50Ω input terminator internally.

Figure 2. AC Test Circuit

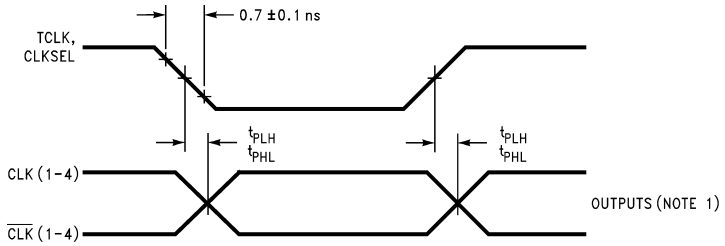


Figure 3. Propagation Delay, TCLK, CLKSEL to Outputs

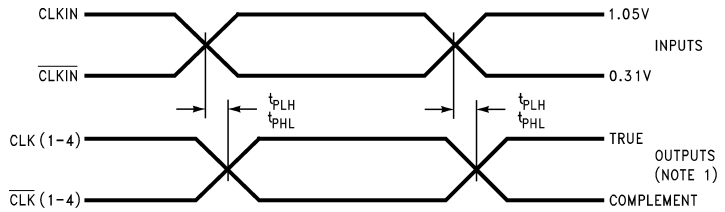
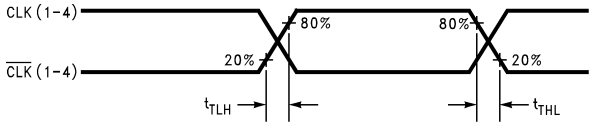


Figure 4. Propagation Delay, CLKIN/$\overline{\text{CLKIN}}$ to Outputs



The output to output skew, which is defined as the difference in the propagation delays between each of the four outputs on any one 100115 shall not exceed 75 ps.

Figure 5. Transition Times

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