National Semiconductor

100315
Low-Skew Quad Clock Driver

General Description

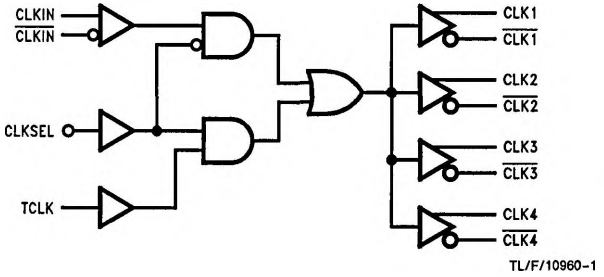
The 100315 contains four low skew differential drivers, designed for generation of multiple, minimum skew differential clocks from a single differential input. This device also has the capability to select a secondary single-ended clock source for use in lower frequency system level testing. The 100315 is a 300 Series redesign of the 100115 clock driver.

Features

- Low output to output skew (≤50 ps)
- Differential inputs and outputs
- Small outline package (SOIC)
- Secondary clock available for system level testing
- 2000V ESD protection
- Voltage compensated operating range: −4.2V to −5.7V
- Military and industrial grades available

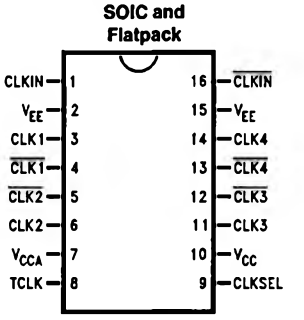
Ordering Code: See Section 5

Logic Diagram



TL/F/10960–1

Connection Diagram



TL/F/10960–2

Pin Names	Description
CLKIN, $\overline{\text{CLKIN}}$	Differential Clock Inputs
CLK_{1-4}, $\overline{CLK}_{1-4}$	Differential Clock Outputs
TCLK	Test Clock Input†
CLKSEL	Clock Input Select†

†TCLK and CLKSEL are single-ended inputs, with internal 50 kΩ pulldown resistors.

Truth Table

CLKSEL	CLKIN	$\overline{\text{CLKIN}}$	TCLK	CLK_N	$\overline{CLK}_N$
L	L	H	X	L	H
L	H	L	X	H	L
H	X	X	L	L	H
H	X	X	H	H	L

L = Low Voltage Level
H = High Voltage Level
X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Plastic	+150°C
Ceramic	+175°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{CC} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Single-Ended Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Single-Ended Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(Min)}$	
I_{IH}	Input High Current					V_{IN} = $V_{IH(Max)}$	
	CLKIN, $\overline{CLKIN}$			150	μA		
	TCLK			250	μA		
	CLKSEL			250	μA		
V_{DIFF}	Input Voltage Differential	150			mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	V_{CC} − 2V		V_{CC} − 0.5V	V		
I_{CBO}	Input Leakage Current	−10			μA	V_{IN} = V_{EE}	
I_{EE}	Power Supply Current	−67		−35	mA		

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Commercial Version (Continued)

AC Electrical Characteristics V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{MAX}	Maximum Clock Frequency	750		750		750		MHz	
t_{PLH} t_{PHL}	Propagation Delay CLKIN, $\overline{CLKIN}$ to $CLK_{(1-4)}$, $\overline{CLK}_{(1-4)}$ Differential Single-Ended	 0.59 0.59	 0.79 0.99	 0.62 0.62	 0.82 1.02	 0.67 0.67	 0.87 1.07	ns	*Figures 1, 3*
t_{PLH} t_{PHL}	Propagation Delay, TCLK to $CLK_{(1-4)}$, $\overline{CLK}_{(1-4)}$	0.50	1.20	0.50	1.20	0.50	1.20	ns	*Figures 1, 2*
t_{PLH} t_{PHL}	Propagation Delay, CLKSEL to $CLK_{(1-4)}$, $\overline{CLK}_{(1-4)}$	0.80	1.60	0.80	1.60	0.80	1.60	ns	*Figures 1, 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	0.80	0.30	0.80	0.30	0.80	ns	*Figures 1, 4*
t_{OST} DIFF	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		50		50		50	ps	(Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Industrial Version

DC Electrical Characteristics V_{EE} = −4.2V to −5.7, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610	mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	
V_{IH}	Single-Ended Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Single-Ended Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = $V_{IL(Min)}$	

Industrial Version (Continued)

DC Electrical Characteristics V_{EE} = −4.2V to −5.7, V_{CC} = V_{CCA} = GND (Continued)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions
		Min	Max	Min	Max		
I_{IH}	Input HIGH Current						
	CLKIN, $\overline{CLKIN}$		107		107	µA	V_{IN} = $V_{IH\ (Max)}$
	TCLK		300		300	µA	
	CLKSEL		260		260	µA	
V_{DIFF}	Input Voltage Differential	150		150		mV	Required for Full Output Swing
V_{CM}	Common Mode Voltage	V_{CC} − 2V		V_{CC} − 0.5V		V	
I_{CBO}	Input Leakage Current	−10		−10		µA	V_{IN} = V_{EE}
I_{EE}	Power Supply Current	−70	−30	−70	−30	mA	

AC Electrical Characteristics V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{MAX}	Maximum Clock Frequency	750		750		750		MHz	
t_{PLH} t_{PHL}	Propagation Delay CLKIN, $\overline{CLKIN}$ to $CLK_{(1-4)}$, $\overline{CLK_{(1-4)}}$								
	Differential	0.59	0.99	0.62	0.82	0.67	0.87	ns	*Figures 1, 3*
	Single-Ended	0.59	0.99	0.62	1.02	0.67	1.07		
t_{PLH} t_{PHL}	Propagation Delay, TCLK to $CLK_{(1-4)}$, $\overline{CLK_{(1-4)}}$	0.50	1.20	0.50	1.20	0.50	1.20	ns	*Figures 1, 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	0.80	0.30	0.80	0.30	0.80	ns	
t_{OST} DIFF	Maximum Skew Opposite Edge Output-to-Output Variation to Output Path		50		50		50	ps	(Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same package device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Military Version—Preliminary

DC Electrical Characteristics V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025		−870	mV	0°C to +125°C	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830		−1620	mV	0°C to +125°C			
		−1830		−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035			mV	0°C to +125°C	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 50Ω to −2.0V	1, 2, 3
		−1085			mV	−55°C			
V_{OLC}	Output LOW Voltage			−1610	mV	0°C to +125°C			
				−1555	mV	−55°C			

Military Version—Preliminary (Continued)

DC Electrical Characteristics V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND (Note 3) (Continued)

Symbol	Parameter	Min	Typ	Max	Units	T_C	Conditions	Notes
V_{DIFF}	Input Voltage Differential	150			mV	−55°C to +125°C	Required for Full Output Swing	1, 2, 3
V_{CM}	Common Mode Voltage	V_{CC} − 2.0		V_{CC} − 0.5	V	−55°C to +125°C		1, 2, 3
V_{IH}	Single-Ended Input High Voltage	−1165		−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs	1, 2, 3, 4
V_{IL}	Single-Ended Input Low Voltage	−1830		−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs	1, 2, 3, 4
I_{IH}	Input HIGH Current CLKIN, $\overline{CLKIN}$			120	µA	−55°C to +125°C	V_{IN} = $V_{IH(Max)}$	1, 2, 3
	TCLK			350	µA			
	CLKSEL			300	µA			
I_{CBO}	Input Leakage Current	−10			µA	−55°C to +125°C	V_{IN} = V_{EE}	1, 2, 3
I_{EE}	Power Supply Current, Normal	−90		−30	mA	−55°C to +125°C		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

AC Electrical Characteristics V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay CLKIN, $\overline{CLKIN}$ to $CLK_{(1-4)}$, $\overline{CLK}_{(1-4)}$	0.61	0.81	0.61	0.81	0.60	0.83	ns	*Figures 1* and *2*	1, 2, 3
t_{PLH} t_{PHL}	Propagation Delay, TCLK to $CLK_{(1-4)}$, $\overline{CLK}_{(1-4)}$	0.50	1.20	0.50	1.20	0.50	1.20	ns		
$t_{S\,G-G}$	Skew Gate to Gate (Note 5)		100		100		100	ps		4
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	0.80	0.30	0.75	0.25	0.75	ns		

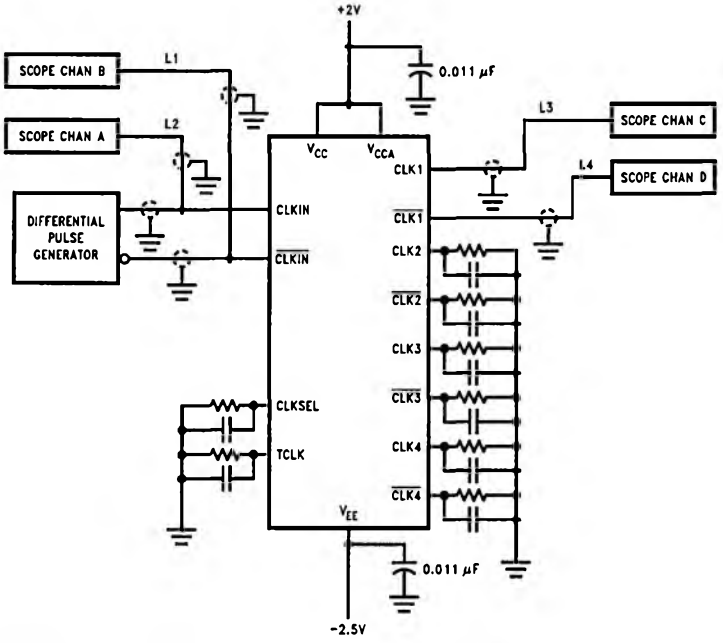
Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C, then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C and −55°C temperature (design characterization data).

Note 5: Maximum output skew for any one device.



TL/F/10960–3

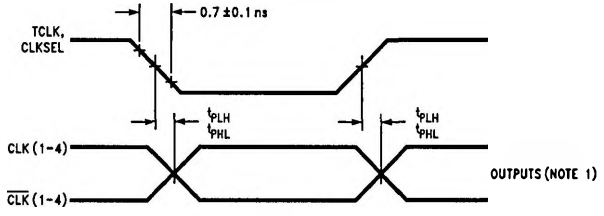
Note 1: Shown for testing CLKIN to CLK1 in the differential mode.

Note 2: L1, L2, L3 and L4 = equal length 50Ω impedance lines.

Note 3: All unused inputs and outputs are loaded with 50Ω in parallel with ≤3 pF to GND.

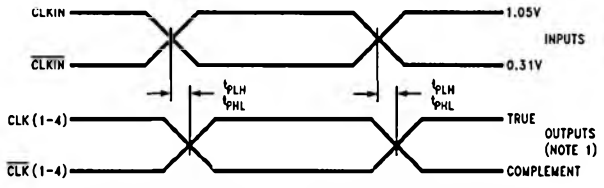
Note 4: Scope should have 50Ω input terminator internally.

FIGURE 1. AC Test Circuit



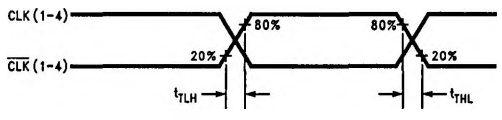
TL/F/10960–4

FIGURE 2. Propagation Delay, TCLK, CLKSEL to Outputs



TL/F/10960–5

FIGURE 3. Propagation Delay, CLKIN/CLKIN to Outputs



TL/F/10960–6

FIGURE 4. Transition Times

Note 1: The output to output skew, which is defined as the difference in the propagation delays between each of the four outputs on any one 100115 shall not exceed 75 ps.