National Semiconductor

ADVANCE INFORMATION

100310
Low Skew 2:8 Differential Clock Driver

General Description

The 100310 is a low skew 8-bit differential clock driver which is designed to select between two separate differential clock inputs. The low output to output skew (< 50 ps) is maintained for either clock input. A LOW on the select pin (SEL) selects CLKINA, $\overline{\text{CLKINA}}$ and a HIGH on the SEL pin selects the CLKINB, $\overline{\text{CLKINB}}$ inputs.

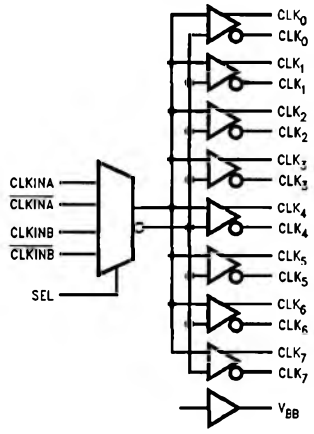
The 100310 is ideal for those applications that need the ability to freely select between two clocks, or to maintain the ability to switch to an alternate or backup clock should a problem arise with the primary clock source.

A V_{BB} output is provided for single-ended operation.

Features

- Low output to output skew (≤ 50 ps)
- Differential inputs and outputs
- Allows multiplexing between two clock inputs
- Voltage compensated operating range: −4.2V to −5.7V

Logic Symbol



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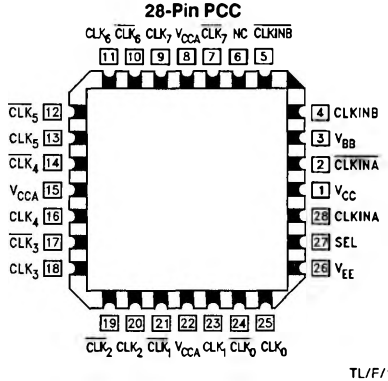
Pin Names	Description
$CLKIN_n$, $\overline{CLKIN}_n$	Differential Clock Inputs
SEL	Select
CLK_{0-7}, $\overline{CLK}_{0-8}$	Differential Clock Outputs
V_{BB}	V_{BB} Output
NC	No Connect

Truth Table

CLKINA	$\overline{\text{CLKINA}}$	CLKINB	$\overline{\text{CLKINB}}$	SEL	CLK_n	$\overline{CLK}_n$
H	L	X	X	L	H	L
L	H	X	X	L	L	H
X	X	H	L	H	H	L
X	X	L	H	H	L	H

Connection Diagram

28-Pin PCC



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